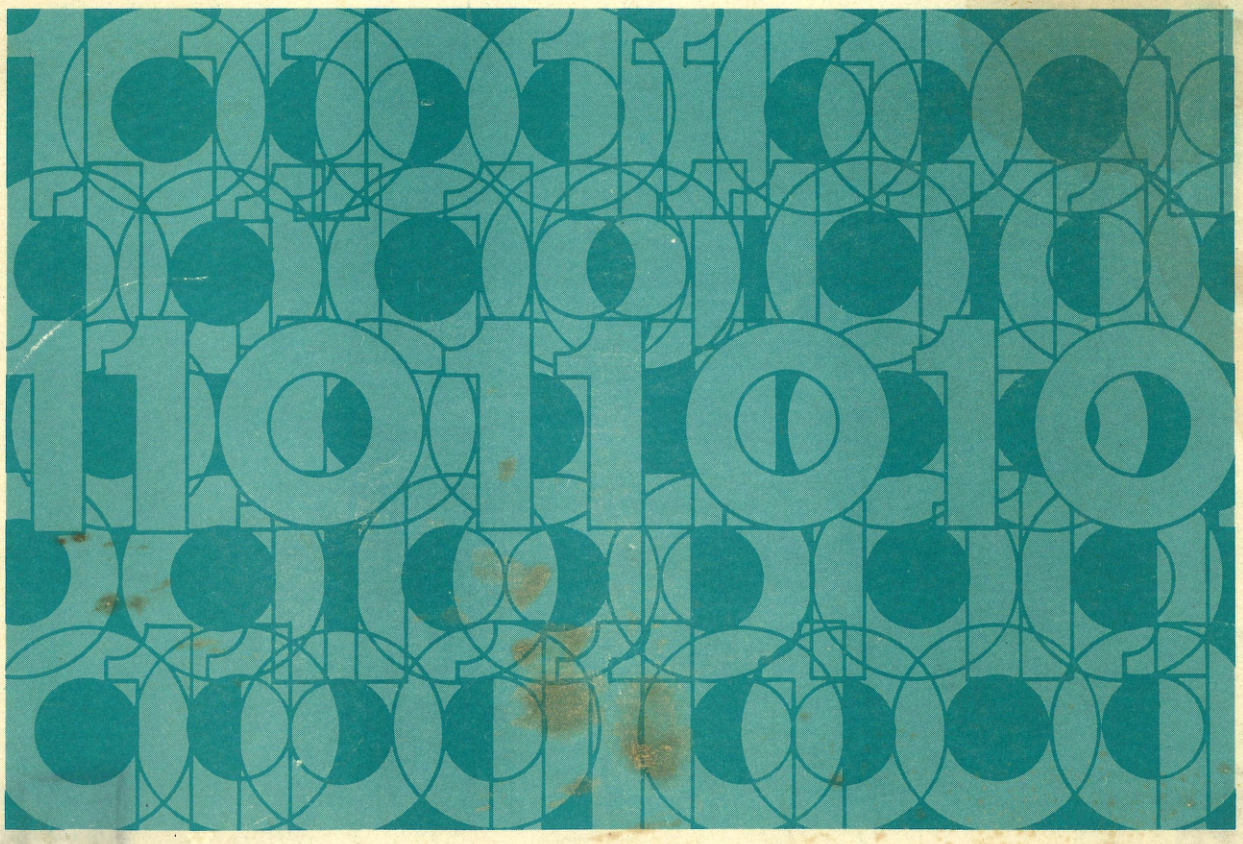
PRICE $4.95
(May be applied towards the purchase of the Model 100A)

INTRODUCTION TO LOGIC ANALYZERS

— BY WAY OF THE MODEL 100A

INCLUDES:

- Basic Logic Analyzer Concepts
- How to use the Controls
- Understanding Circuit Operation
- Assembly & Test of the Model 100A Kit
- Troubleshooting
- Microcomputer and other Applications



PARATRONICS, INC.

WARNING

THIS INSTRUMENT IS DESIGNED FOR USE WITH A 3-WIRE AC SYSTEM (3RD WIRE = SAFETY GROUND). BYPASSING THIS SAFETY GROUND IS NOT RECOMMENDED. IN THE EVENT OF AN INTERNAL FAILURE, SERIOUS INJURY OR DEATH MAY RESULT DUE TO ELECTRICAL SHOCK. TROUBLESHOOTING OF THIS INSTRUMENT SHOULD BE PERFORMED BY EXPERIENCED TECHNICAL PERSONNEL ONLY.

CAUTION

THIS INSTRUMENT IS PROVIDED WITH AN ADJUSTABLE BLANKING OUTPUT VOLTAGE WHICH CAN BE SET AS HIGH AS +30 VOLTS. MAKE SURE THAT THIS VOLTAGE IS ADJUSTED TO A LEVEL COMPATIBLE WITH THE RECOMMENDATIONS OF THE MANUFACTURER OF YOUR SCOPE BEFORE CONNECTING IT; OTHERWISE DAMAGE TO THE SCOPE'S BLANKING CIRCUIT MAY RESULT. REFER TO SECTION 7.0 OF THIS MANUAL FOR ADDITIONAL INFORMATION.

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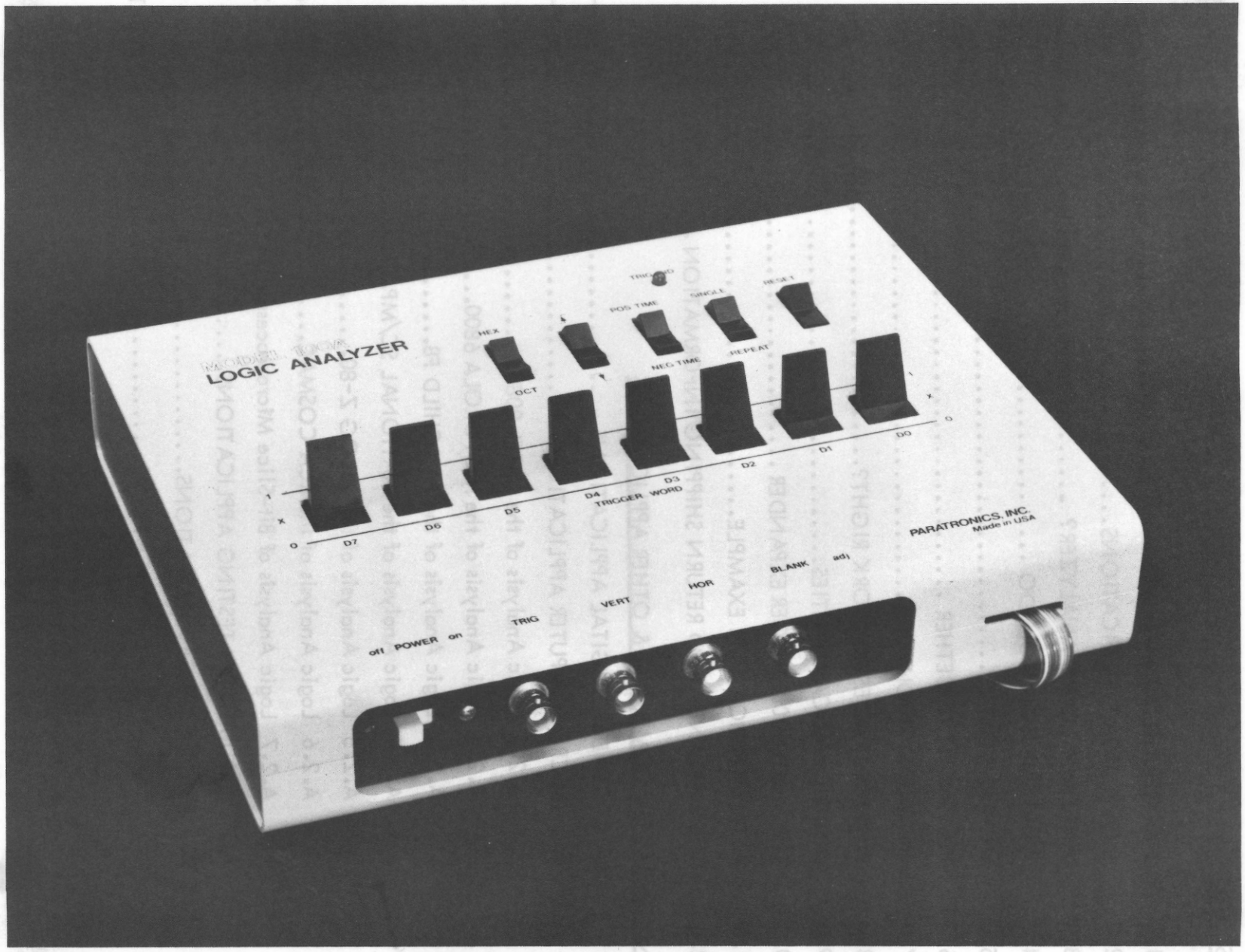

The Model 100A Logic Analyzer

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1.0 INTRODUCTION

From the early computer days, there's a story told about a Computer Wizard who secretly loaded in a routine which drove the other programmers wild. At random intervals, this routine would automatically activate itself and print out the following message: "I AM THE ELUSIVE GLITCH...CATCH ME IF YOU CAN!" Then it would reset, disappear deep into the memory of the machine, and patiently wait for the next unsuspecting moment before activating again. There was no way to find it.

Individuals involved in today's complex digital systems know all too well that the "elusive glitch" or other troubles such as stuck bits, timing problems, improper instructions, etc., can occur even without the help of the Computer Wizard. And for troubleshooting these problems, many engineers and technicians have found that their oscilloscopes suffer from several serious shortcomings:

1. A scope can only look at a few bits at a time--it doesn't have an means for displaying or triggering on the data words of microprocessors, memories, counters, logic arrays, and other common digital devices.

2. A scope can only display events after it's triggered; but if you're triggering on the problem itself, such as an unwanted branch in a program, it's highly desirable to be able to "look back in time" and view the events leading up to the problem.

3. An ordinary nonstorage oscilloscope is incapable of displaying and holding a "snapshot" of a one-time sequence of events for later analysis. Such events are typical of computers, peripherals, controllers, and other aperiodic systems.

A new instrument has been devised to circumvent these shortcomings: The Logic Analyzer. Still in its infancy, this instrument is already changing the way microprocessors and other digital systems are being designed and tested. And, as we shall see in the sections that follow, the logic analyzer not only resolves the above deficiencies of the ordinary oscilloscope, but it also has several other unique features which make it ideal for a wide range of system development, troubleshooting, production testing, field service, and educational applications.

This manual explains the general concept of logic analysis as well as the assembly, test, principles of operation and varied applications of the Model 100A Logic Analyzer. The Model 100A is a high-quality instrument which has many characteristics and features that are comparable with other commercial units except one: It's a lot lower in cost. And because of this, the logic analyzer is now within the reach of engineering companies, hobbyists, schools, and others who previously could not afford or justify the high cost of other models.

A very similar unit, the Model 100 Logic Analyzer (cover story, February 1977 issue of Popular Electronics) was the first unit developed in the Model 100 series. The Model 100A, described in this manual, is an improved version of that first unit. (We took advantage of the delay of several months between the time the construction article was first submitted and the date of publication to include several significant improvements including: better switches, a more ruggedized and simply constructed case, and a larger power supply to power a variety of accessories that enhance the capabilities of the instrument.)

Since the Model 100A differs in construction from the Model 100, the information contained in this manual supersedes all other published descriptions. Furthermore, Paratronics, Inc. reserves the right to incorporate additional design changes without notice--at any time--in order to improve this product.

If you have any questions or comments, we'd like to hear from you. Address all correspondence to:

Paratronics, Inc.
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Los Gatos, CA. 95030

2.0 MODEL 100A SPECIFICATIONS

DISPLAY TYPE	TRUTH TABLE
DISPLAY FORMAT	HEXADECIMAL & OCTAL
DATA COLLECTION MODES	POSITIVE & NEGATIVE TIME
TRIGGER WORD	8 BITS WIDE--EXPANDABLE TO 26 BITS*
TRIGGER SWITCHES	3 POSITION: "1," "0," "X" (DON'T CARE)
TRIGGER INDICATORS	LED ON FRONT PANEL, ALSO TRIGGER WORD APPEARS INTENSIFIED IN TRUTH TABLE
TRIGGER OUTPUT	AUXILIARY PULSE WHICH OCCURS WHEN VALID TRIGGER WORD IS DETECTED. USE AS SCOPE SYNC PULSE FOR TROUBLE-SHOOTING.
TRIGGER BUS	AVAILABLE AT PROBE INPUT
TRIGGER OR CLOCK DELAY	0 - 999 EVENTS*
DISPLAY SIZE	1 BYTE (8 BITS) X 16 WORDS DEEP--EXPANDABLE TO 3 BYTES (24 BITS)*
INPUT LOAD	360 µA (LOGIC 0)
INPUT THRESHOLD	TTL WITH HYSTERESIS (APPROX. 1.6 VOLTS)
INPUT LOGIC LEVELS	-0.5V to +15V (TTL, DTL, CMOS, & MOS)
DATA COLLECTION RATE	GREATER THAN 8 MEGABYTES/SEC.
DATA SET-UP TIME	10 ns BEFORE ACTIVE CLOCK EDGE
DATA HOLD TIME	15 ns AFTER ACTIVE CLOCK EDGE
INPUT CLOCK	POSITIVE OR NEGATIVE EDGE TRIGGERING
BLANKING OUTPUT	ADJUSTABLE TO +30V
OSCILLOSCOPE COUPLING	AC/DC
POWER	115 VAC, 60Hz; LESS THAN 7.5 WATTS (230 VAC, 50Hz also available.)
WEIGHT	5 POUNDS

*FEATURES AVAILABLE USING MODEL 10 TRIGGER EXPANDER

3.0 WHAT IS A LOGIC ANALYZER?

That's a difficult question. For such a new instrument in the test equipment field, it's suprising how many different models with varying features and performance already exist. So, before we discuss the two main types of analyzers, let's first describe this unique instrument by considering how you would modify an ordinary oscilloscope so that it offered some of the features of a typical logic analyzer. Here's what you'd have to do:

1. Add storage capability. (Analyzers have a data memory so that they can take a "snapshot" of the operation of the circuit and display it indefinitely.)

2. Add 8 or more input channels and tie them to 8 or more corresponding CRT beams. (Most logic analyzers can display 8 or more channels simultaneously.)

3. Turn the timebase generator "inside out" so you can trigger backwards in time. (Analyzers usually have a "negative time" feature which allows the events leading up to a trigger to be displayed; by contrast, an ordinary scope can only show you the events after the trigger.)

Obviously, the first modification would be costly. Modification #2 would be a mechanical monstrosity. And Modification #3 is downright impossible. A simpler way would be to leave your scope as is and connect it to a device which contains multiple-channel inputs, a data memory, and display circuitry; i. e., a logic analyzer.

So, what are the functions of a logic analyzer? An analyzer:

1. Captures data in an internal memory and provides refresh logic for a steady display of a computer's program flow or other sequence of digital events.

2. Acquires data through 8 or more independent, buffered, input probes.

3. Has a pre-trigger acquisition mode which provides a "negative time" display of the events leading up to a trigger.

In addition, logic analyzers generally provide the following features:

1. Repetitive or "moving picture" display of sequences of digital events.

2. Eight or more 3-position control switches with possible settings of "1," "0," and "X" (don't care) for each bit of a trigger word.

3. Post-trigger, or "positive time" display of data.

There are basically two types of logic analyzers on the market today: The logic state analyzer and the logic timing analyzer. Both have the general features described above. However, the logic state analyzer differs from the logic timing analyzer in the way captured data are presented. The state analyzer displays data in the "truth table" or "data domain" format shown in figure 3-1, while the timing analyzer displays it as a synthetic timing diagram as shown in the same figure. Another difference is that the timing analyzer usually has an asychronous data collection mode, i.e., it can collect events that occur between the system's normal clocked states. By contrast, the state analyzer utilizes the system clock and therefore operates only in a synchronous mode. Thus, the advantage of the timing diagram approach is that it can sometimes be used to detect glitches that occur between the normal clocked states; the disadvantage is that it's a lot harder to interpret the display when you're tracing program flow.

Individuals have been known to violently disagree in their preferences for one type of analyzer or the other; but one point is generally agreed upon: In the hands of an adept user, both types of instruments can usually perform the same functions. For example, the state analyzer can be used to locate glitches by utilizing the TRIG output signal, which provides a sync pulse when the pre-set trigger word occurs. Thus, after locating a mis-set bit or other problem, the user can set the trigger word to the logic state just prior to the problem and utilize the TRIG output to trigger his scope. Then, with his scope in the normal analog mode, he simply probes the circuit to determine whether a glitch, race condition, or other problem was responsible for the erroneous logic state.

Similarly, a user who becomes familiar with the synthetic timing diagram can learn to transpose the display into a sequence of 1's and 0's for tracing program flow.

In summary, most experts agree that both state and timing analyzers have their place in supporting the development and debugging of computers or other complex digital systems, but that the logic state analyzer alone is more useful for maintenance, troubleshooting, production testing, and just plain understanding the operation of digital equipment.

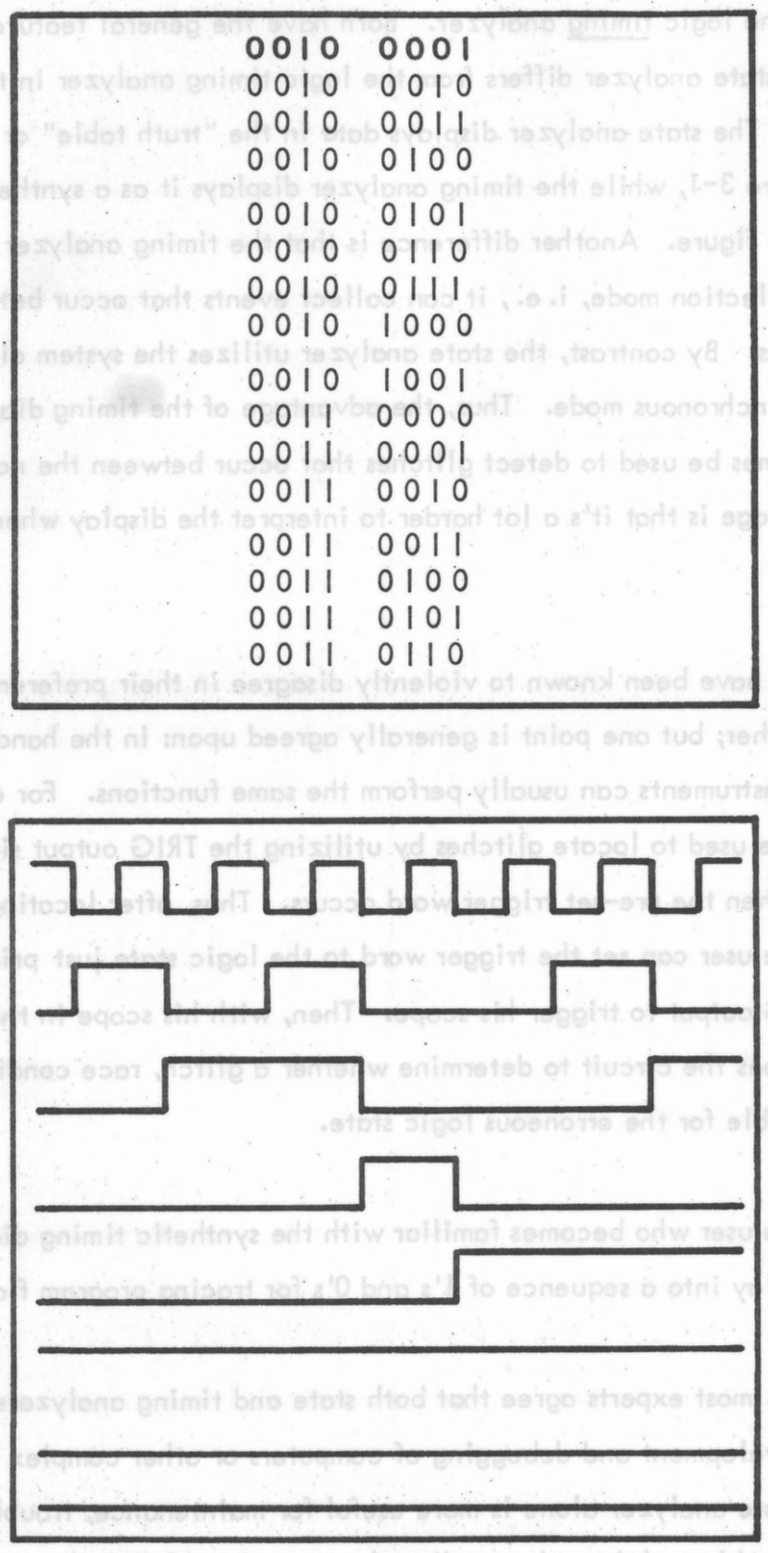


FIG. 3-1. Logic analyzer display methods.

The Model 100A is, of course, a state analyzer; and specific details of its wide-ranging applications are described in the Appendix and elsewhere in this manual. However, as a preview, a partial list of applications is provided below. The Model 100A may be used for:

1. Understanding and troubleshooting microprocessor address, instruction, and data flow.
2. Examining the contents of ROM'S.
3. Tracing the operation of control logic.
4. Checking counter and shift register operation.
5. Monitoring I/O sequences.
6. Verifying proper system operation during production testing.
7. Field service.
8. Educational applications.

4.0 THE CONTROLS OF THE MODEL 100A

The controls of the Model 100A are shown in the photograph in the front of the manual. Here's what they do:

TRIGGER WORD SWITCHES - These are 3-position switches which you may use to pre-set the trigger word, which can be up to 8 bits wide. Choose "0," "1," or "X" (don't care) for each bit of the trigger word. If "X" is selected for all bit positions and if 16 or more clock pulses occur, the analyzer will collect and display whatever data appear on the input probes, i.e., without the requirement for a specific trigger word. This feature is particularly useful when you have a problem to analyze but you don't know exactly where to trigger. Simply take a set of random "snapshots" and examine the data flow until you capture a suspicious event.

HEX/OCTAL SELECT - Use this switch to select the display format in accordance with your application. For example, the hexadecimal mode is best for monitoring the 4-bit sequences associated with binary and BCD counters. (See figure 4-1.) On the other hand, the octal mode is ideally suited for tracing programs written in an octal code, such as the INTEL 8080 ADD and STORE program of figure 4-2.

POS/NEG TIME SELECT - With this switch in the positive time position, the analyzer will display the trigger word intensified at the top of the truth table, with the next 15 logic states listed in sequence below. (Again see figure 4-1.) Use this mode, for example, to examine the contents of a PROM starting with a known word at location 0. (A counter is required to increment the address of the PROM.) On the other hand, in the negative mode, the trigger word is intensified at the bottom of the display and the prior 15 words are listed above. Thus, if you were tracing the steps of a program leading to a branch address as shown in figure 4-2, this is the mode you would use.

SINGLE/REPEAT SELECT - The single mode provides a continuously displayed "snapshot" of the truth table. Use this feature if you want to capture a "one-time" sequence of events and keep it displayed until you've finished with your analysis. Alternatively, the repeat mode gives you a "moving picture" type of display where captured truth tables are continously overlaid so you can watch individual bits change or ripple as a function of time. This feature can be handy when you're monitoring repetitive sequences (such as those which occur when your program is in a loop) and you're trying to catch the "illusive glitch."

RESET - This control is used in the single mode to clear the display and "arm" the analyzer for the capturing of the next truth table. Thus, the reset switch is directly analogous to the single-shot control found on many scopes.

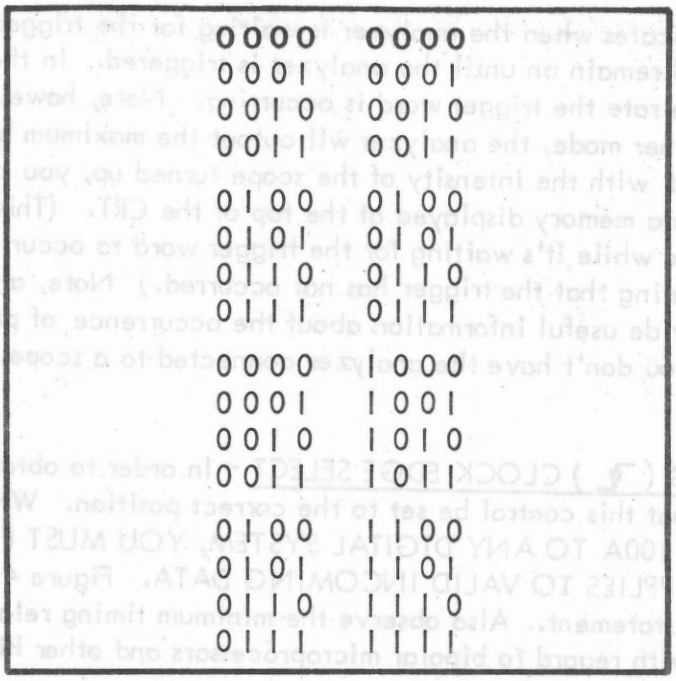


FIG. 4-1. Hexadecimal format of logic analyzer. Right side of truth table is output of "good" 4-bit counter; left side is output of another counter with MSB stuck at "0." Trigger word (0000 0000) is intensified at top of truth table for positive time mode.

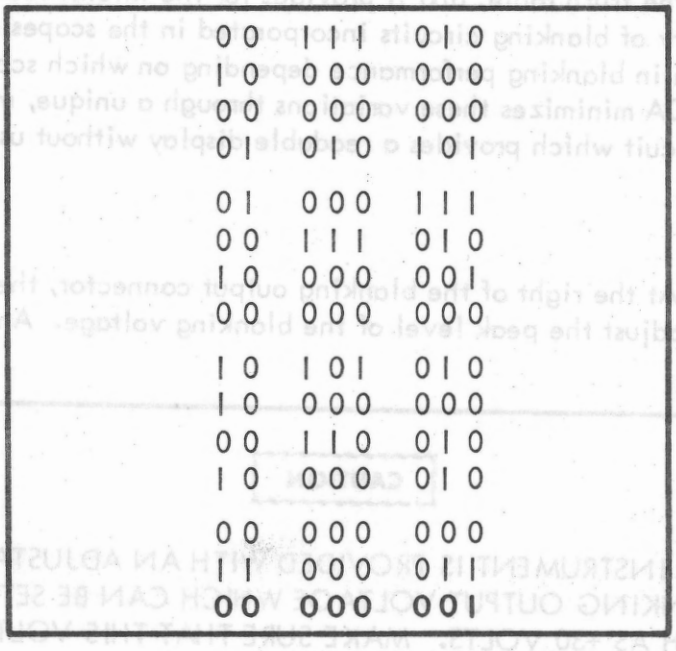


FIG. 4-2. Octal format. Truth table shows the steps of an Intel 8080 ADD and STORE program leading up to a branch instruction. Trigger word (00 000 001) is the branch address and is shown at bottom of truth table for negative time mode.

TRIG IND - This LED indicates when the analyzer is waiting for the trigger word to occur. In the single mode, it will remain on until the analyzer is triggered. In the repeat mode, the LED will illuminate at the rate the trigger word is occurring. Note, however, while waiting for the trigger word in either mode, the analyzer wll output the maximum blanking voltage that it's adjusted to. And with the intensity of the scope turned up, you still may see one or two locations of the data memory displayed at the top of the CRT. (This is the normal starting point for the logic while it's waiting for the trigger word to occur and it provides yet another way of indicating that the trigger has not occurred.) Note, also, that the LED trigger indicator can provide useful information about the occurrence of particular instructions or logic states--even if you don't have the analyzer connected to a scope.

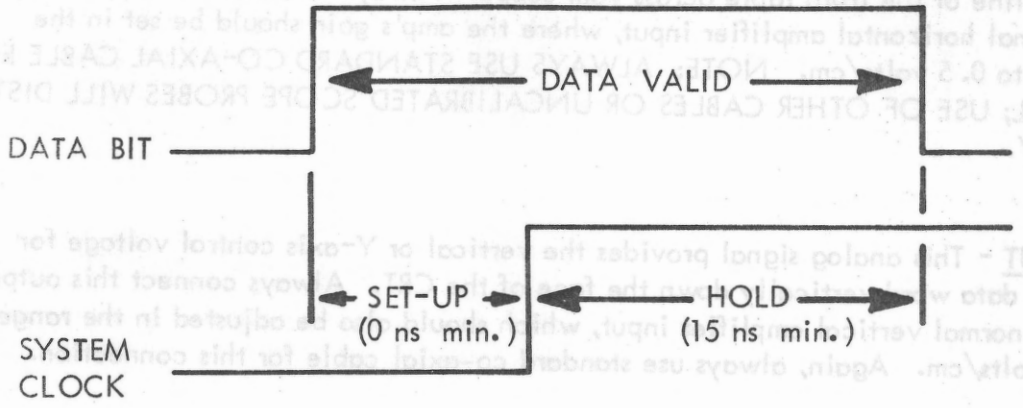
RISING (⌐)/FALLING (¬) CLOCK EDGE SELECT - In order to obtain a meaningful display, it is important that this control be set to the correct position. WHENEVER YOU CONNECT THE MODEL 100A TO ANY DIGITAL SYSTEM, YOU MUST FIRST DETERMINE WHICH CLOCK EDGE APPLIES TO VALID INCOMING DATA. Figure 4-3 explains the importance of the above statement. Also observe the minimum timing relationships shown in the figure, particularly with regard to bipolar microprocessors and other high-speed digital circuits.

BLANK OUTPUT - This "tri-level" output provides up to +30 volts of blanking signal which is connected to the Z-axis, intensity modulation, or blanking input of your scope. The blanking signal serves two purposes: It turns the CRT beam off at the appropriate intervals between displayed characters in the truth table, and it provides for the intensification of the trigger word. Due to the variety of blanking circuits incorporated in the scopes on the market today, you'll notice a variation in blanking performance depending on which scope you're using. However, the Model 100A minimizes these variations through a unique, microprogrammed character generating circuit which provides a readable display without using the blanking signal at all!

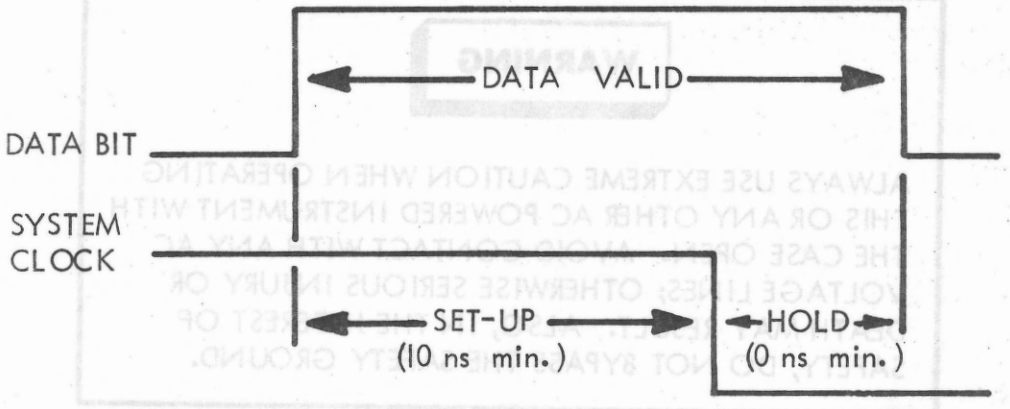
BLANKING ADJUST - At the right of the blanking output connector, there is an access hole through which you can adjust the peak level of the blanking voltage. And as it says in the front of the manual:

CAUTION

THIS INSTRUMENT IS PROVIDED WITH AN ADJUSTABLE BLANKING OUTPUT VOLTAGE WHICH CAN BE SET AS HIGH AS +30 VOLTS. MAKE SURE THAT THIS VOLTAGE IS ADJUSTED TO A LEVEL COMPATIBLE WITH THE RECOMMENDATIONS OF THE MANUFACTURER OF YOUR SCOPE BEFORE CONNECTING IT; OTHERWISE DAMAGE TO THE SCOPE'S BLANKING CIRCUIT MAY RESULT. REFER TO SECTION 7.0 OF THIS MANUAL FOR ADDITIONAL INFORMATION.



POSITIVE CLOCK EDGE SYSTEMS



NEGATIVE CLOCK EDGE SYSTEMS

FIG. 4-3. Proper input clock edge must be chosen in order to collect meaningful data.

In other words, if you're in a hurry and you're not sure if the blanking voltage is set for the scope you're using... DON'T CONNECT IT UP! (Basically, all you'll lose is the intensification of the trigger word.)

HOR OUTPUT - This analog signal provides the horizontal or X-axis control voltage for writing each line of the truth table across your scope. Always connect this output to your scope's external horizontal amplifier input, where the amp's gain should be set in the range of 0.2 to 0.5 volts/cm. NOTE: ALWAYS USE STANDARD CO-AXIAL CABLE FOR THIS SIGNAL; USE OF OTHER CABLES OR UNCALIBRATED SCOPE PROBES WILL DISTORT THE DISPLAY.

VERT OUTPUT - This analog signal provides the vertical or Y-axis control voltage for writing each data word vertically down the face of the CRT. Always connect this output to your scope's normal vertical amplifier input, which should also be adjusted in the range of 0.2 to 0.5 volts/cm. Again, always use standard co-axial cable for this connection.

TRIG OUTPUT - As was discussed in the last section, the trigger output provides a sync pulse every time the trigger word occurs. This feature is extremely useful for microprocessor troubleshooting of noise, timing, or intermittent problems which occur during--or between--particular logic states.

POWER SWITCH - This switch, located to the left of the TRIG output, turns the Model 100A on and off.

WARNING

ALWAYS USE EXTREME CAUTION WHEN OPERATING THIS OR ANY OTHER AC POWERED INSTRUMENT WITH THE CASE OPEN. AVOID CONTACT WITH ANY AC VOLTAGE LINES; OTHERWISE SERIOUS INJURY OR DEATH MAY RESULT. ALSO, IN THE INTEREST OF SAFETY, DO NOT BYPASS THE SAFETY GROUND.

INPUT DATA PROBES - The input probes are constructed out of a multi-colored flat ribbon cable containing ten wires. Each wire is terminated in a "universal" pin connector and has the signal-carrying functions defined in figure 4-4. The probe tips will interface directly with standard wire wrap pins and IC clips; but they're easily adaptable for use with "E-Z hooks" and ball clips, if your particular application so requires.

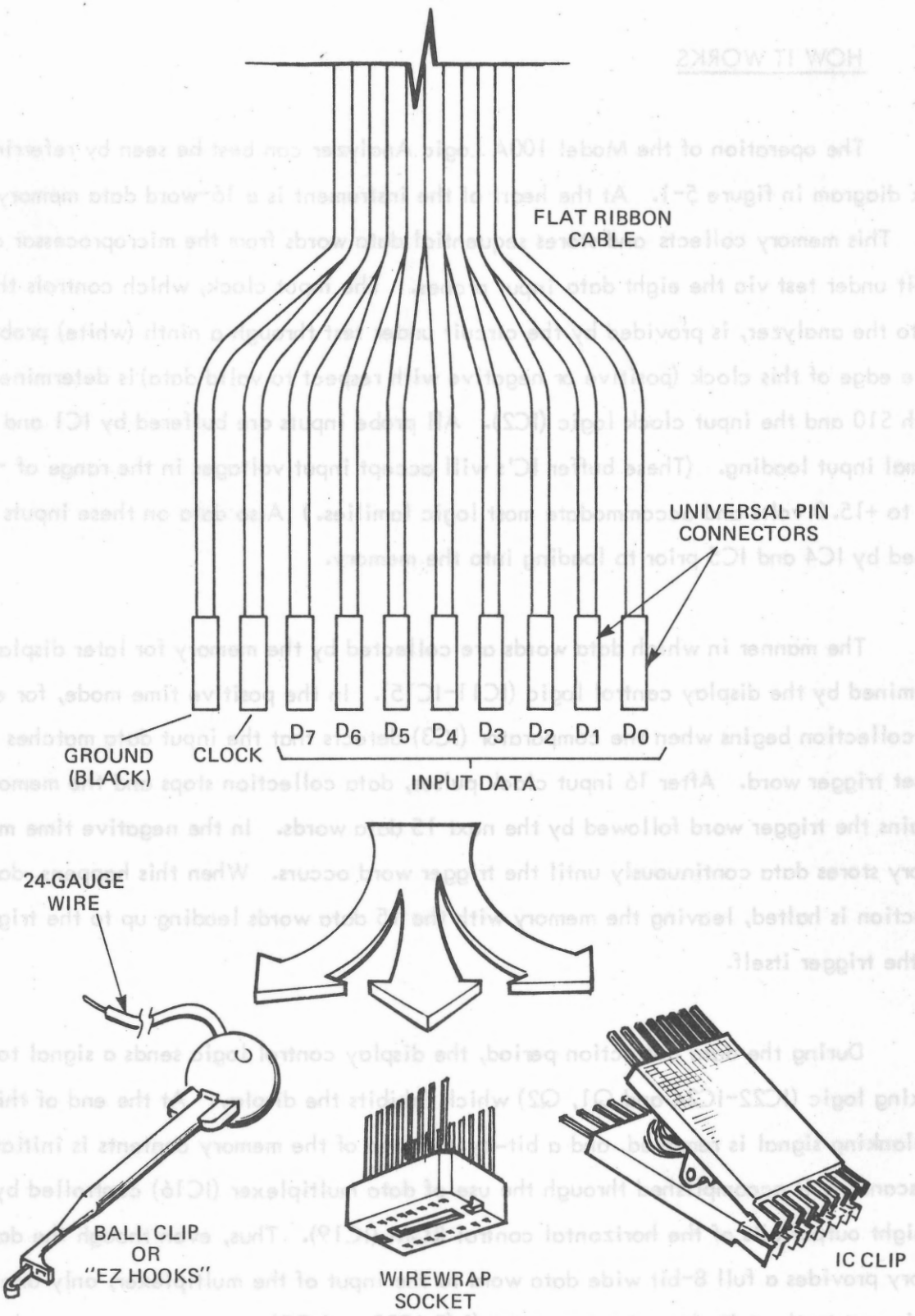


FIG. 4-4. Data Probe Interfacing Techniques.

5.0 HOW IT WORKS

The operation of the Model 100A Logic Analyzer can best be seen by referring to the block diagram in figure 5-1. At the heart of the instrument is a 16-word data memory (IC6, IC7). This memory collects and stores sequential data words from the microprocessor or logic circuit under test via the eight data input probes. The input clock, which controls the data rate to the analyzer, is provided by the circuit under test through a ninth (white) probe. The active edge of this clock (positive or negative with respect to valid data) is determined by switch S10 and the input clock logic (IC2). All probe inputs are buffered by IC1 and IC2 for minimal input loading. (These buffer IC's will accept input voltages in the range of -0.5 volts to +15.0 volts and accommodate most logic families.) Also data on these inputs are latched by IC4 and IC5 prior to loading into the memory.

The manner in which data words are collected by the memory for later display is determined by the display control logic (IC11-IC15). In the positive time mode, for example, data collection begins when the comparator (IC3) detects that the input data matches the pre-set trigger word. After 16 input clock pulses, data collection stops and the memory contains the trigger word followed by the next 15 data words. In the negative time mode, the memory stores data continuously until the trigger word occurs. When this happens, data collection is halted, leaving the memory with the 15 data words leading up to the trigger, plus the trigger itself.

During the data collection period, the display control logic sends a signal to the blanking logic (IC22-IC24 and Q1, Q2) which inhibits the display. At the end of this period, the blanking signal is removed, and a bit-by-bit scan of the memory contents is initiated. This scanning is accomplished through the use of data multiplexer (IC16) controlled by three of the eight output bits of the horizontal control ROM (IC19). Thus, even though the data memory provides a full 8-bit wide data word to the input of the multiplexer, only one bit at a time is sent to the 1/0 character generator (1/2 IC20 and Q3).

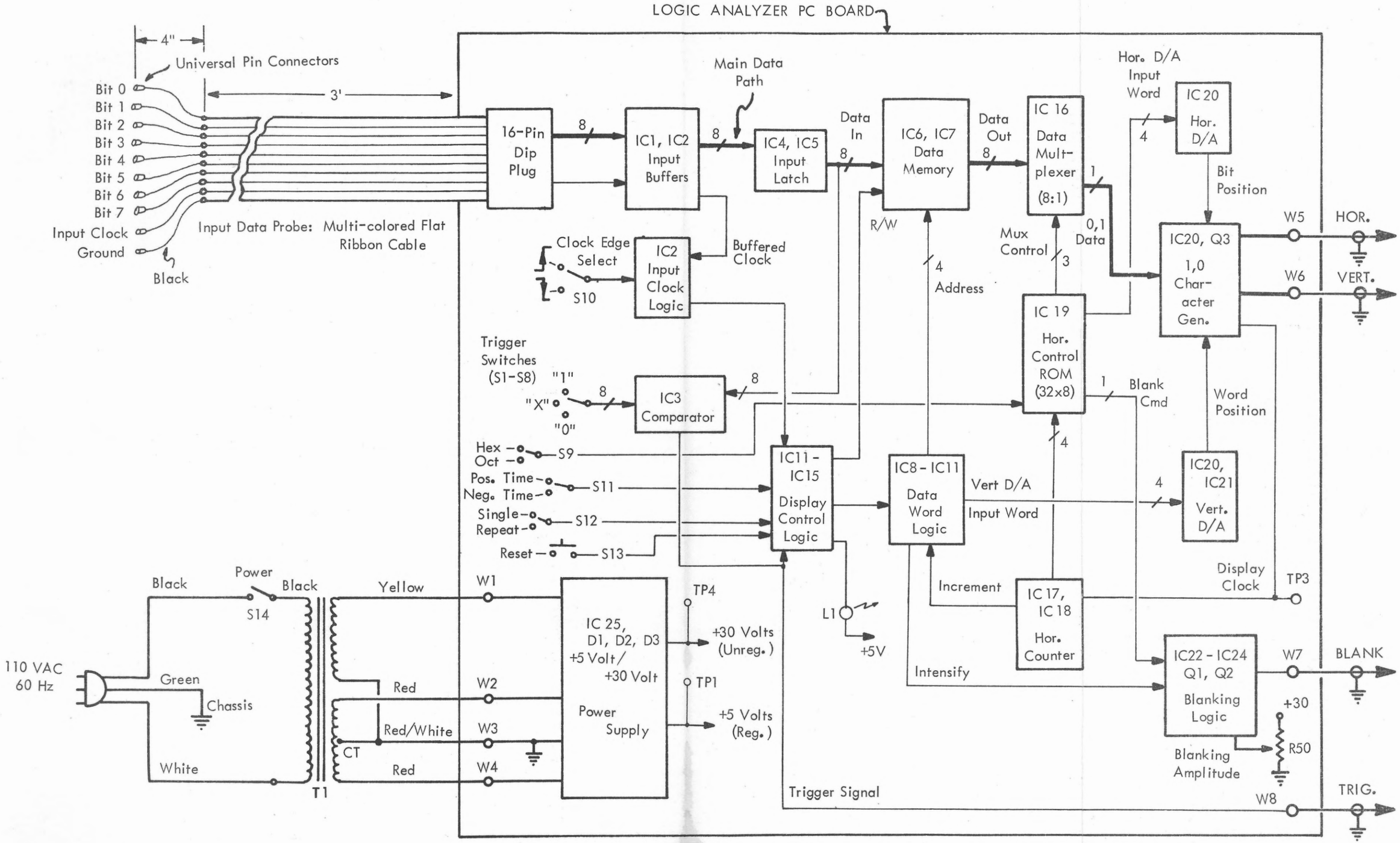
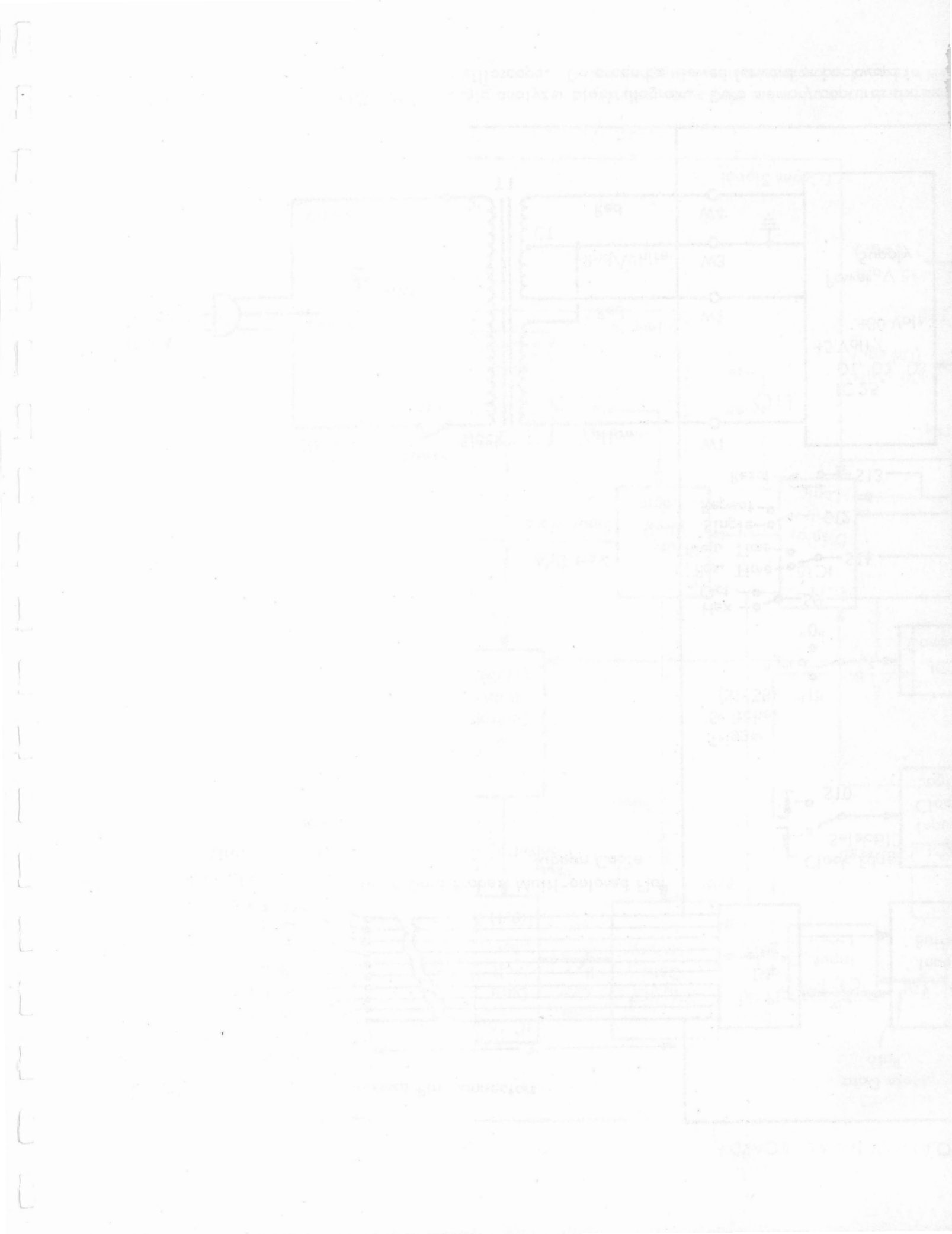


FIG. 5-1. Logic analyzer block diagram. Data memory captures sixteen 8-bit words for truth table display on ordinary oscilloscope. Data can be viewed forward or backward in time with respect to a predetermined trigger word.



The 1/0 character generator circuit then uses this information (together with the CRT beam positioning signals from the horizontal D/A (1/4 IC20) and the vertical D/A (1/4 IC20, IC21) to write a "1" or "0" at the proper location on the screen.

The horizontal D/A receives its digital input information from 4 bits of the horizontal control ROM. The ROM itself receives address information from the horizontal control counter (IC17, IC18): It is the incrementing of this counter which causes the beam to move from right to left across the face of the CRT as the data word is written out.

When the last bit is displayed, the horizontal counter "rolls over" to zero and sends an increment signal to the data word logic (IC8-IC11) which causes the address of the data memory to advance to the next word location. At the same time, the data word logic issues a command to the vertical D/A which causes the beam to move down one row in preparation for the display of the next word. This process continues until all 16 words have been written on the screen. (The horizontal and vertical D/A outputs are shown in Section 7.0, figures 7-2 and 7-3, respectively.)

If the analyzer is in the SINGLE mode, the display control logic prevents the data memory from collecting new data so that the same information is written on the screen. The writing speed is fast enough so that a flicker-free "snapshot" of the contents of the memory is displayed on the CRT. This "snapshot" will remain displayed until the RESET button is pushed, illuminating the trigger indicator LED and arming the analyzer for the capture of another 16-word set of data.

In the REPEAT or "moving picture" mode, the display control logic provides an automatic reset after the display of each 16-word truth table.

Blanking between displayed bits is provided by the remaining bit of the horizontal control ROM. (Note that this ROM is performing three separate functions: control of the data multiplexer, control of the horizontal D/A, and blanking control. The use of a ROM

as a controller is called "microprogramming," an efficient design technique often used in high-level computers.) An intensify command from the data word logic permits the trigger to appear brighter than the other data words.

Finally, a trigger pulse (TRIG) is generated from the comparator for external use each time the trigger word occurs. The resulting output pulse can be connected to the sync input of a scope when it is necessary to look at a specific signal which is a function of the incoming trigger word. This is a powerful troubleshooting feature which permits the user to "home" in on the glitch or timing problem responsible for an illegal logic state.

6.0 PUTTING IT TOGETHER

The exploded view of the Model 100A in figure 6-3 shows how easily the unit goes together. And since all active components are tested before the kit leaves the factory, you shouldn't have any difficulty in getting the analyzer to work properly as long as you carefully follow the step-by-step instructions in this section. In fact, it's a good idea to first familiarize yourself with the assembly steps and the associated parts of the Model 100A before you begin. Also, for your convenience, here's a list of the tools you'll need and some hints on their proper usage with regard to the assembly of the Model 100A.

1. Low-power soldering station such as a Weller Model W-TCP, including moist sponge for wiping the tip: Use a small tip on the soldering iron and periodically clean it by wiping it on the moist sponge. When soldering, use 60/40 rosin core solder ONLY. Never, NEVER use acid core or externally applied fluxes. Also, never allow the tip to remain in contact with the PC board for more than 10 seconds. If you're not getting a shiny solder joint after applying the tip of the iron and the solder for a few seconds, then something must be wrong with the iron or solder you're using. (The Model 100A PC board is specially treated so that the solder should flow quickly and easily.)

2. Small-to-medium size pair of pliers: The hardest step in the assembly of the Model 100A is probably the insertion of the power cord strain relief into the back of the case. In step 29, you'll use the pliers to squeeze the strain relief around the cord as tight as you can and force it into its mounting hole. (BUT BE CAREFUL NOT TO MAR THE CASE DURING THIS OPERATION.)

3. Medium-size flat head screwdriver: All screws should be tightened so that they're snug--but it's not necessary to overtighten anything.

4. Hex wrench set: The easiest way to install the power supply transformer, the voltage regulator, and the BNC connectors is to use hex wrenches. If these are not available, use the pliers described above, but be sure you're able to tighten the parts securely without damaging anything.

5. Small pair of wire cutters: Use these to trim the leads of all resistors, capacitors, transistors, diodes, etc., after soldering. It's not necessary to trim the leads of any of the IC's.

6. Small pair of long nose pliers: Use these to carefully make the bends required to install the resistors and similar components. (You can make this job a lot easier if you have one of those commonly available wedge-shaped, plastic lead bending tools.)

7. An inexpensive, 2X magnifying glass: This is a great way to inspect solder joints. Scan the board systematically and you'll be surprised what kinds of potential problems even a low-cost, low-power, magnifying glass can uncover for you.

8. Silicon grease: This improves the thermal contact between the voltage regulator, heat sink, and copper clad area of the PC board. Silicon grease is available in small tubes at most retail electronic parts stores.

9. Patience: This is the most useful tool of all. If you take your time and inspect each step along the way, you'll save yourself a lot of grief later.

Misc. Assembly Hints - Before you begin, consider the following general hints which will assist you in performing the assembly of the PC board:

1. Use the Parts List to identify all components.

2. "Color in" components as you locate them in the assembly drawings of figure 6-1 and 6-2.

3. Install all resistors so that the tolerance band is toward the right for all those that are horizontally-oriented; and facing toward the bottom of the board for all those that are vertically-oriented. This will help you to rapidly identify resistor values for later checkout and trouble-shooting.

4. Install all components of the same height at one time. Then lay a piece of cardboard or other flat material over the components to hold them in place as you turn the PC board over for soldering.

The parts list for the Model 100A is shown next. If you find any discrepancies or damaged components prior to assembly, contact your dealer directly, or write to Paratronics, Inc. describing your problem so we can take the appropriate action.

MODEL 100A PARTS LIST

C1--2200-μF, 16-volt electrolytic capacitor

C2--220-μF, 50-volt electrolytic capacitor

C3--20-μF, 50-volt electrolytic capacitor

C4, C5--150--pF ceramic disc capacitor, 10% tolerance

C6--15pF ceramic disc capacitor, 10% tolerance

C7, C8, C9, C10--0.1-μF, 12-volt ceramic disc capacitor, 20% tolerance

C11--300pF ceramic disc capacitor, 10% tolerance

C12--180 pF ceramic disc capacitor, 10% tolerance

C13--0.01μF ceramic disc capacitor, 20% tolerance

D1, D2, D3--rectifier diode, 1.0-amp, 100PIV (IN4002 or similar)

IC1, IC2--74LS14 hex inverter IC with Schmidt-trigger inputs (do not substitute; use Fairchild only)

IC3--74S15 triple 3-input AND gate IC with open collector outputs

IC4, IC5, IC9--74LS175 quad latch IC (use Fairchild only)

IC6, IC7--7489 RAM IC (16x4)

IC8--74LS161 4-bit synchronous counter IC

IC10--74LS83 4-bit adder IC

IC11, IC12, IC22--7400 quad 2-input NAND gate IC

IC13, IC14, IC18--74LS73 dual JK flip flop IC (do not substitute)

IC15--7473 dual JK flip flop IC (do not substitute)

IC16--74LS151 8-to-1 multiplexer IC

IC17--74LS90 decade counter IC

IC19--8223 256-bit PROM with open collector outputs (also 6330-1 may be used)

IC20--LM3900 quad current amplifier IC

IC21--7407 hex buffer IC with open collector outputs

IC23--74LS21 dual 4-input AND gate IC

IC24--7406 hex inverter IC with open collector outputs

IC25--LM309K 5-volt regulator IC

Q1, Q3--2N3904 NPN silicon transistor

Q2--2N3905 PNP silicon transistor

MODEL 100A PARTS LIST
(con't)

The following resistors are 1/4-watt, 5% tolerance:

- R1 through R27--4700 ohms
- R28--3300 ohms
- R29--470 ohms
- R30--1000 ohms
- R31, R32, R33--8200 ohms
- R34, R35, R36--2700 ohms
- R37--1800 ohms
- R38--2000 ohms
- R39, R40--33,000 ohms
- R41, R42--56,000 ohms
- R43, R44, R45--22,000 ohms
- R46, R47--24,000 ohms
- R48, R49--130,000 ohms
- R51, R52--180 ohms
- R53--47,000 ohms
- R54, R55--11,000 ohms

The following resistors are 1/4-watt, 2% tolerance:

- R56--4700 ohms
- R57--2400 ohms
- R58--5100 ohms
- R59--2700 ohms
- R50--5000-ohm trimmer potentiometer (Spectrol 43P502 or similar)
- S1 through S8--double-pole 3-position PC-mounted switch
- S9 through S12--Dpdt PC-mounted switch
- S13--momentary-action Dpst PC-mounted switch
- S14--Spst switch (panel mount)
- L1--light-emitting diode (HP5082-4860 or similar)
- T1--dual-winding power transformer with 16-volt CT and 22-volt winding
- J1-J4--BNC connectors (panel mount)

Misc.--~~Line cord~~, strain relief, ~~mounting hardware~~, 3 ~~feet of Spectra Strip~~ multicolored flat ribbon cable ~~(26 guage)~~, ~~DIP sockets~~, ~~16-pin flat ribbon DIP plug~~, ~~heat sink for voltage regulator~~, hookup wire, solder, ~~case and mounting brackets~~, ~~shrink tubing~~, pin connectors, etc.

STEP	PROCEDURE	FIGURE
	Steps 1-8 apply to the assembly of the "IC Side" of the PC Board:	
( ) 1.	Mount and solder all resistors in place on the side of the board labeled "IC SIDE." Before soldering, be sure that all resistors are properly located. Also, don't use 5% tolerance resistors in locations where 2% resistors are specified; otherwise the appearance of the display will be affected. Hint: Make sure R24 is not inserted in the feedthru hole which is located near its pads. Also, the trimmer pot, R50, is not installed until step 10.	6-1
( ) 2.	Mount and solder rectifier diodes D1, D2, and D3 in place. Be sure that their polarities are correct.	6-1
( ) 3.	Mount and solder all IC's except input buffers IC1 and IC2, which require sockets. (Use of sockets for the PROM (IC19) and the quad current amp (IC20) is recommended but not essential.) Before soldering, be certain that all IC's are oriented properly.	6-1
( ) 4.	Mount and solder the IC sockets. You should have one 16-pin socket left over for the flat ribbon DIP plug associated with the input probes. This socket is mounted on the other side of the board--do not install it at this time.	6-1
( ) 5.	Mount and solder transistors Q1, Q2, and Q3. (You'll have to spread the leads apart slightly.) Be sure and observe transistor type and polarity. (As you hold the board with the cutout at the upper left, Q1 and Q2 are mounted with their flat edges towards you; Q3 is mounted with its flat edge to your right.) Note: Some kits contain transistor packages which do not have this flat edge. Instead, they have a circular-type package with small flat surface to indicate the emitter. If you have this type of package, locate the small flat surface and install the package so that this surface is nearest the label "e" in the assembly drawing.	6-1
( ) 6.	Mount and solder all capacitors except C1 (2200 μF). Be sure and observe the polarities of C2 (220 μF) and C3 (10 μF) before soldering.	6-1
( ) 7.	Install and solder jumper wire, J1, near C13 (0.01μf), which is located near the upper right-hand-side of the board.	6-1

STEP	PROCEDURE	FIGURE
( ) 8.	THIS COMPLETES THE ASSEMBLY OF THE IC SIDE OF THE BOARD. BEFORE CONTINUING, CLIP OFF ALL EXCESS LEAD LENGTHS AND INSPECT ALL COMPONENTS FOR CLEAN, SHINY SOLDER JOINTS AND PROPER ORIENTATION. ALSO LOOK FOR SOLDER BRIDGES AND LEADS NOT SOLDERED. (A 2X MAGNIFIER WORKS WONDERS FOR THIS TYPE OF INSPECTION.)	6-1
	Steps 9-18 apply to the assembly of the "SWITCH SIDE" of the PC Boards:	
( ) 9.	Turn the PC board over so that the "SWITCH SIDE" is facing up, and the cutout is towards the upper right.	6-2
( ) 10.	Mount and solder the 16-pin DIP socket for the input probes. Also mount and solder the blanking voltage adjustment pot, R50. (There are extra pads for R50: make sure that the pads used permit the front of R50 to line up with the edge of the PC board. Also, the pins of R50 may have a snug fit with the holes in the board.)	6-2
( ) 11.	Mount and solder the large filter capacitor C1 (2200 µF), observing the polarity indicated in figure 6-2.	6-2
( ) 12.	Coat both top and bottom of the heat sink with a light layer of silicon grease (available at most retail electronic parts stores). Also coat the bottom of the voltage regulator case and the mating surface of the PC board.	6-4
( ) 13.	Mount the voltage regulator and the heat sink to the PC board using the 4-40 hardware provided. (The side of the voltage regulator near the corner of the PC board is secured by a 4-40 screw and a hex nut temporarily; later the hex nut will be removed and discarded in favor of a threaded standoff when the board is mounted into the case.) Now solder the voltage regulator leads in place.	6-4
( ) 14.	Mount the following rocker switches: S9 (HEX/OCT), S10 (CLOCK EDGE SELECT), S11 (POS/NEG TIME), and S12 (SINGLE/REPEAT). NOTE: BEFORE SOLDERING IN PLACE, MAKE CERTAIN THAT THESE SWITCHES ARE SEATED ALL THE WAY DOWN AND ARE PERPENDICULAR TO THE PC BOARD; OTHERWISE, THE TOP OF THE CASE WILL NOT MATE PROPERLY. (Hint: Hold the board vertically as you solder the switches in place.)	6-2

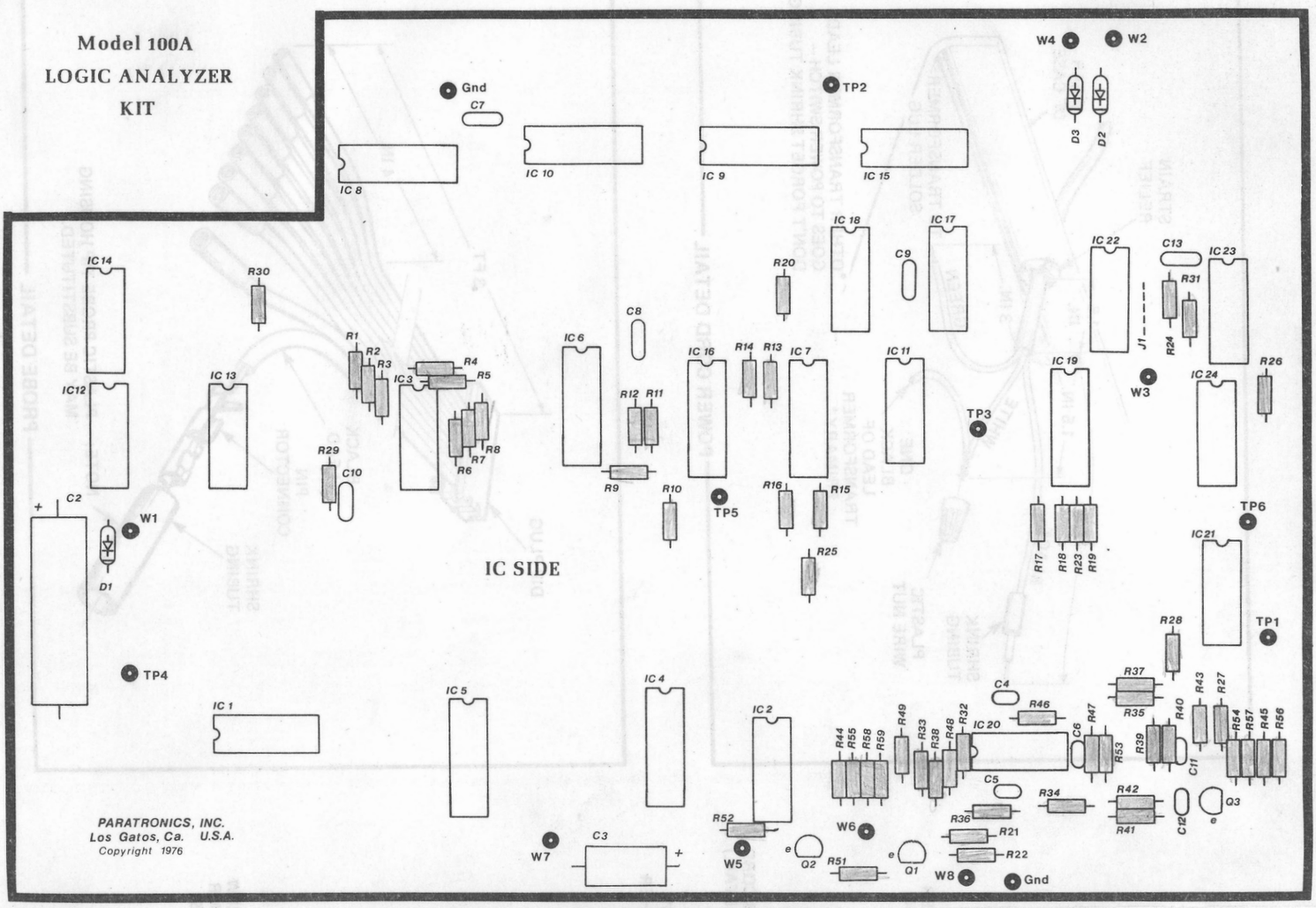


FIG. 6-1. IC side component layout.

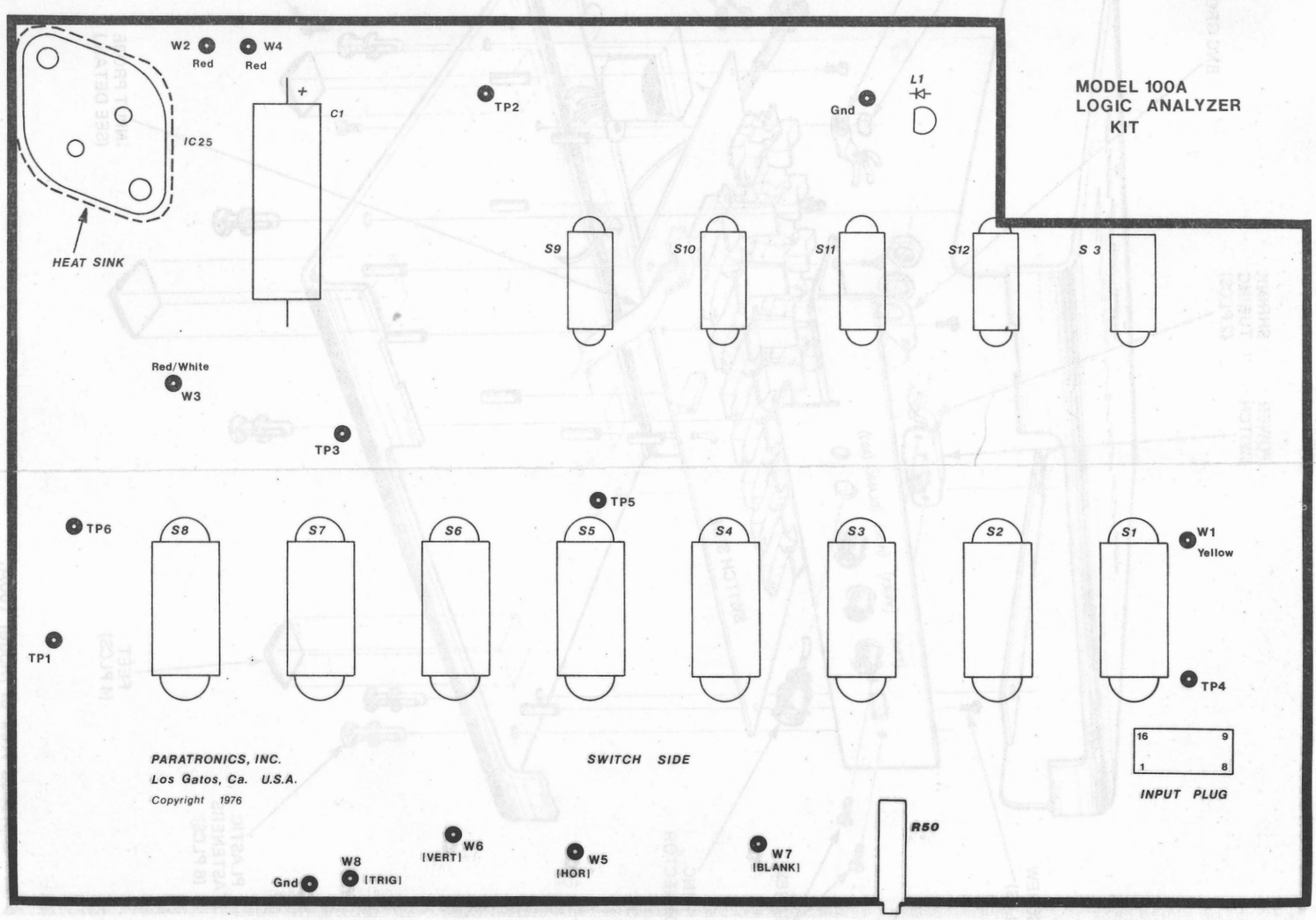


FIG. 6-2. Switch side component layout.

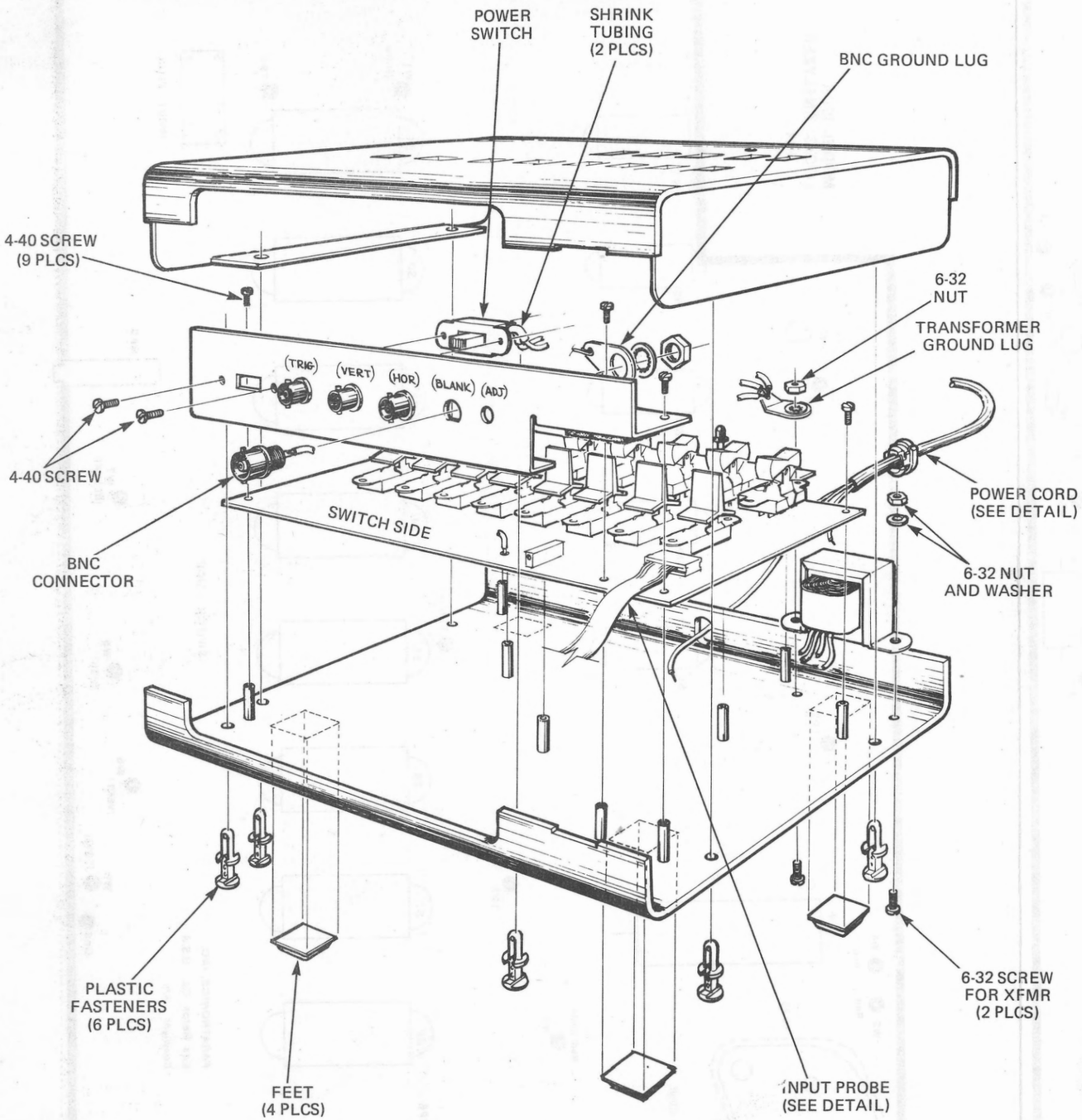
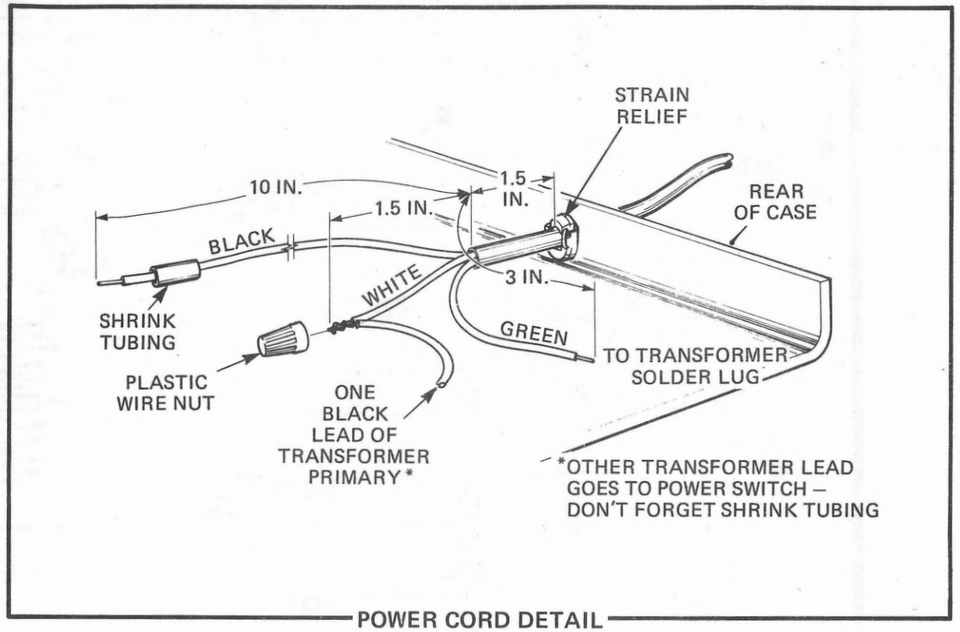
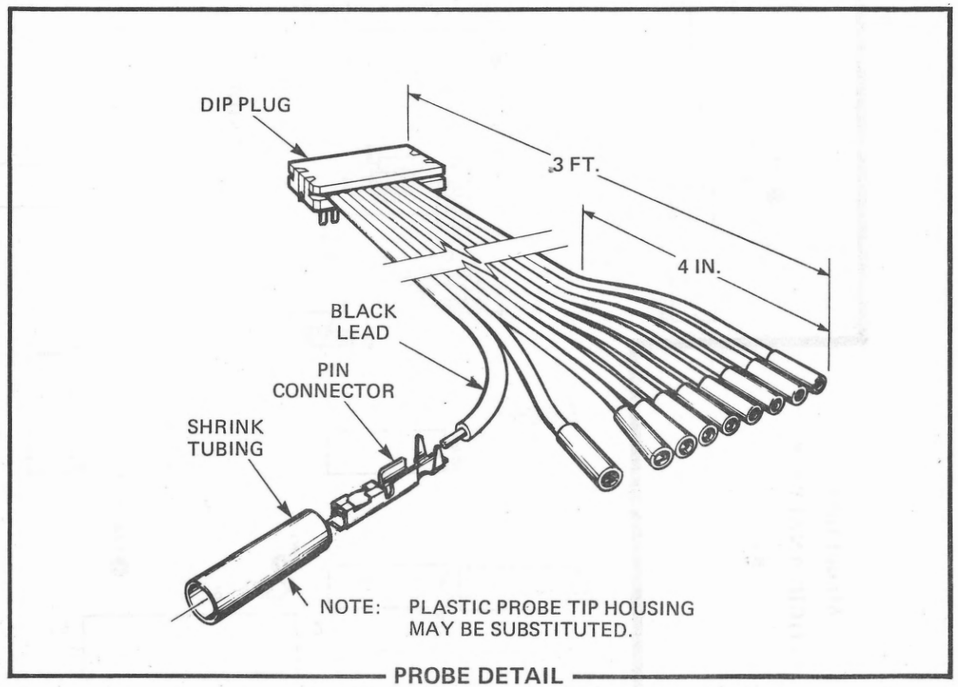


FIG. 6-3. Exploded view of Model 100A.



POWER CORD DETAIL



PROBE DETAIL

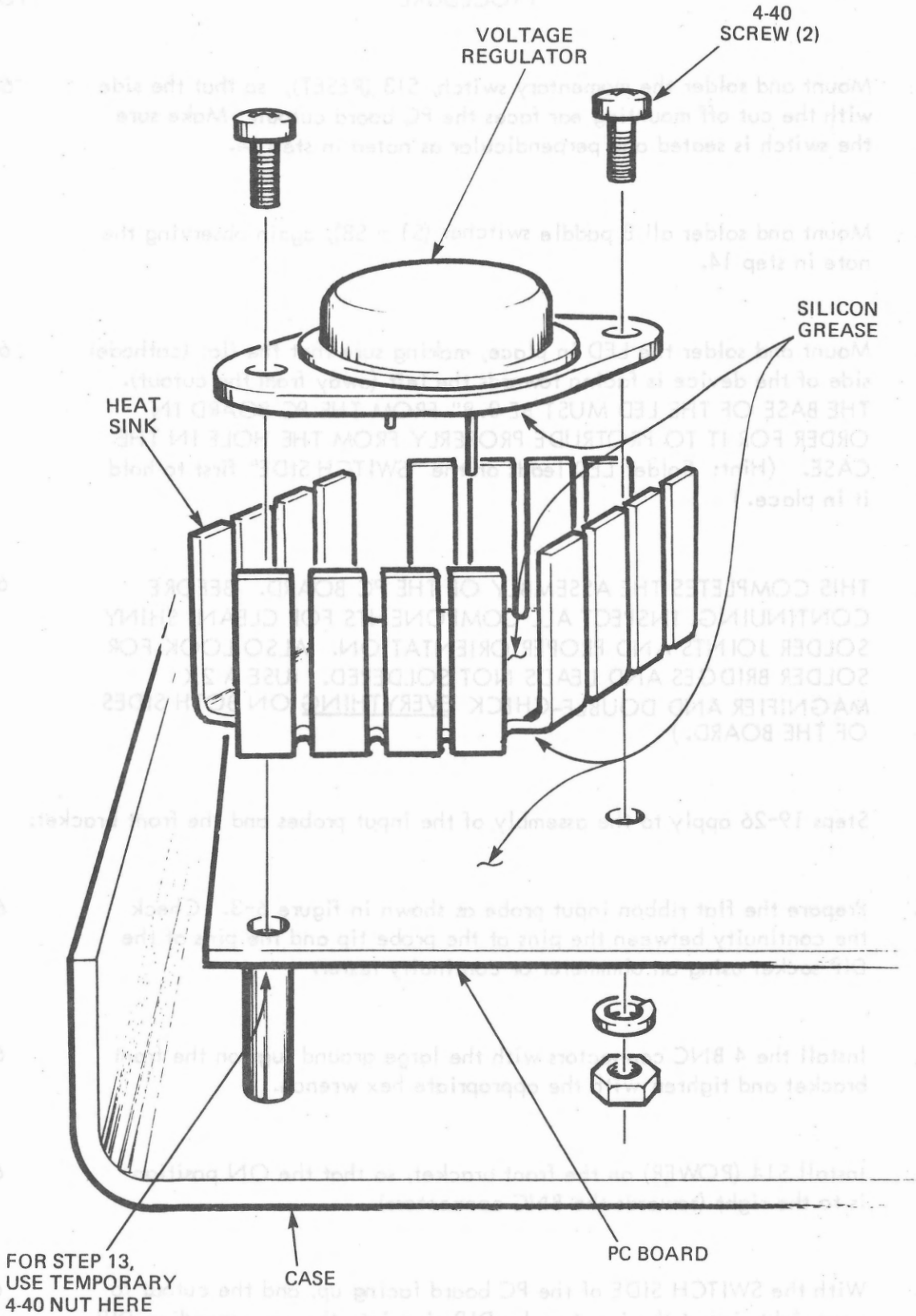


FIG. 6-4. Voltage regulator and heat sink assembly detail.

STEP	PROCEDURE	FIGURE
( ) 15.	Mount and solder the momentary switch, S13 (RESET), so that the side with the cut off mounting ear faces the PC board cutout. Make sure the switch is seated and perpendicular as noted in step 14.	6-2
( ) 16.	Mount and solder all 8 paddle switches (S1 - S8), again observing the note in step 14.	
( ) 17.	Mount and solder the LED in place, making sure that the flat (cathode) side of the device is facing towards the left (away from the cutout). THE BASE OF THE LED MUST BE 0.8" FROM THE PC BOARD IN ORDER FOR IT TO PROTRUDE PROPERLY FROM THE HOLE IN THE CASE. (Hint: Solder LED leads on the "SWITCH SIDE" first to hold it in place.)	6-2
( ) 18.	THIS COMPLETES THE ASSEMBLY OF THE PC BOARD. BEFORE CONTINUING, INSPECT ALL COMPONENTS FOR CLEAN, SHINY SOLDER JOINTS AND PROPER ORIENTATION. ALSO LOOK FOR SOLDER BRIDGES AND LEADS NOT SOLDERED. (USE A 2X MAGNIFIER AND DOUBLE-CHECK <u>EVERYTHING</u> ON BOTH SIDES OF THE BOARD.)	6-2
	Steps 19-26 apply to the assembly of the input probes and the front bracket:	
( ) 19.	Prepare the flat ribbon input probe as shown in figure 6-3. Check the continuity between the pins at the probe tip and the pins at the DIP socket using an ohmmeter or continuity tester.	6-3
( ) 20.	Install the 4 BNC connectors with the large ground lugs on the front bracket and tighten with the appropriate hex wrench.	6-3
( ) 21.	Install S14 (POWER) on the front bracket, so that the ON position is to the right (towards the BNC connectors).	6-3
( ) 22.	With the SWITCH SIDE of the PC board facing up, and the cutout to your right, insert the input probe DIP plug into the corresponding DIP socket. The black ground connection of the multi-colored probe cable should be to your left.	6-3

STEP	PROCEDURE	FIGURE
( ) 23.	Wire the 4 BNC ground lugs together with a piece of bare bus wire. Solder the free end of this wire to the pad labeled "GND" at the lower, left hand-side of the board. (Insert the wire with the SWITCH SIDE facing up and solder on the "IC SIDE.")	6-3
( ) 24.	Connect a 1" piece of hookup wire from the solder post on the left most BNC connector (TRIG) (near the power switch) to the pad on the PC board labeled "W8."	6-2
( ) 25.	Using 1" wires, connect the adjacent BNC connectors (VERT, HOR, and BLANK) to pads W6, W5, and W7, respectively.	6-2
( ) 26.	THIS COMPLETES THE ASSEMBLY OF THE FRONT BRACKET. MAKE SURE THAT ALL COMPONENTS ARE MECHANICALLY SECURE AND THAT THE SOLDER JOINTS ARE INSPECTED, AND THAT ALL HOOK-UP WIRE CONNECTIONS GO TO THE PROPER PADS ON THE PC BOARD.	6-3
	Steps 27-40 apply to the wiring of the Model 100A:	
( ) 27.	Install the 4 press-on feet to the bottom of the case to protect the finish in the following steps. It's also a good idea to place a cloth or foam material between the finished parts and your work area for additional protection of the finish.	6-3
( ) 28.	Prepare the 3-wire power cord as shown in figure 6-3.	6-3
( ) 29.	Using the strain relief, install the power cord into the rear of the lower half of the case, making sure that the black lead of the cord reaches all the way to the front of the case with at least an inch to spare. (The insulation of the power cord should protrude about 1.5" into the interior of the case as shown in figure 6-3.) NOTE: CONSIDERABLE INSERTION FORCE WILL BE REQUIRED TO INSTALL THE STRAIN RELIEF. TO AVOID DAMAGING THE FINISH ON THE CASE, MASK OFF THE AREA AROUND THE STRAIN RELIEF HOLE WITH MASKING TAPE. Then, using a pair of pliers, tightly close the strain relief around the power cord, align it with the cutout in the rear of the case, and push it in. Good luck.	6-3

STEP	PROCEDURE	FIGURE
( ) 30.	Install the transformer with the two black primary leads facing towards the rear of the case. Make sure you install a ground lug between the nut and the left-hand mounting ear.	6-3
( ) 31.	Connect the green lead of the power cord to the transformer ground lug, but do not solder at this time.	6-3
( ) 32.	Connect the RED/WHITE striped (center tap) lead of the transformer to the transformer ground lug; again, do not solder.	6-3
( ) 33.	Prepare an 8" length of hookup wire and connect one end to the transformer ground lug. Now solder all 3 wires in place.	6-3
( ) 34.	Holding the PC board and front bracket assembly with the SWITCH SIDE facing up, feed the other end of the 8" hookup wire into the pad labeled "W3," located near the center, left side of the board. Insert the wire from the IC SIDE of the board, and solder it to the pad on the SWITCH SIDE.	6-2
( ) 35.	Repeat step 34, soldering the YELLOW transformer lead to the pad labeled "W1," located near the right, center of the board.	6-2
( ) 36.	Repeat step 34, soldering one each of the two remaining RED transformer leads to pads labeled "W2" and "W4," respectively. (Both pads are located near the voltage regulator.)	6-2
( ) 37.	Twist the WHITE power cord bare lead together with the shorter of the two BLACK transformer primary leads. Solder the connection and install a "twist-type" plastic "wire nut." MAKE SURE THE WIRE NUT IS SECURELY FASTENED, AND THAT THERE ARE NO BARE AC WIRES EXPOSED.	6-3
( ) 38.	Place a piece of shrink tubing over the remaining long BLACK transformer primary lead and slide it back away from the bare end. Then solder this lead to the center terminal of the power switch on the front bracket assembly. Be sure and route this wire along the IC SIDE of the board. After soldering, slip the shrink tubing over the power switch terminal and gently heat the tubing with your soldering iron tip to shrink it in place. (Note: Too much heat will melt the solder.)	6-3

STEP	PROCEDURE	FIGURE
( ) 39.	Repeat step 38 using the BLACK power cord lead to the right-hand terminal of the power switch (near the BNC connectors.) MAKE CERTAIN THERE ARE NO EXPOSED AC CONNECTIONS.	6-3
( ) 40.	THIS COMPLETES ALL OF THE REQUIRED WIRING. AS USUAL, CHECK ALL MECHANICAL CONNECTIONS AND ALL SOLDER JOINTS BEFORE CONTINUING. USE YOUR MAGNIFYING GLASS TO MAKE CERTAIN THAT THERE ARE NO SOLDER BRIDGES ON THE PC BOARD, PARTICULARLY WITH REGARD TO THE PADS CONTAINING THE TRANSFORMER LEADS.	

Your Model 100A is now ready for checkout. Please go to the next section in the manual before installing the PC board into the case.

The remaining steps complete the assembly of the Model 100A:

( ) 41.	Remove the hex nut from the voltage regulator mounting screw nearest the corner of the PC board.	6-3
( ) 42.	With the SWITCH SIDE facing up, align the PC board and front bracket assembly to the corresponding holes in the stand-offs attached to the bottom of the case.	6-3
( ) 43.	Loosely install the mounting screws. (Hint: Use your long nose pliers to "start" the screw for the voltage regulator and screw between the paddle switches.) Then install the top cover to check alignment. Move the PC board slightly, as required, to assure that the paddle and rocker switches move freely. Also, gently move the LED as required, so that it protrudes through the hole in the case. When all switches are free to move, tighten down the PC board. Then double-check switch and LED alignment by re-installing the top cover.	6-3
( ) 44.	Secure the bottom of the front bracket assembly to the case by first inserting two plastic female receptacles. Then insert the male fasteners. (The front bracket may have to be moved forward or backward slightly to obtain correct alignment.)	6-3

STEP	PROCEDURE	FIGURE
( ) 45.	Install the top cover using four plastic fastener sets which mate the side plates to the bottom of the case.	6-3

NOTE: The male plastic fasteners used in the above steps may be easily removed by prying underneath the head using a small pocket knife or small flat head screwdriver. HOWEVER, USE CAUTION WHEN REMOVING THESE FASTENERS TO AVOID CUTTING YOURSELF OR DAMAGING THE FINISH OF THE CASE. The fasteners may be reused many times if you use care in removing them.

* * *

THIS COMPLETES THE ASSEMBLY OF THE MODEL 100A

7.0 CHECKING IT OUT

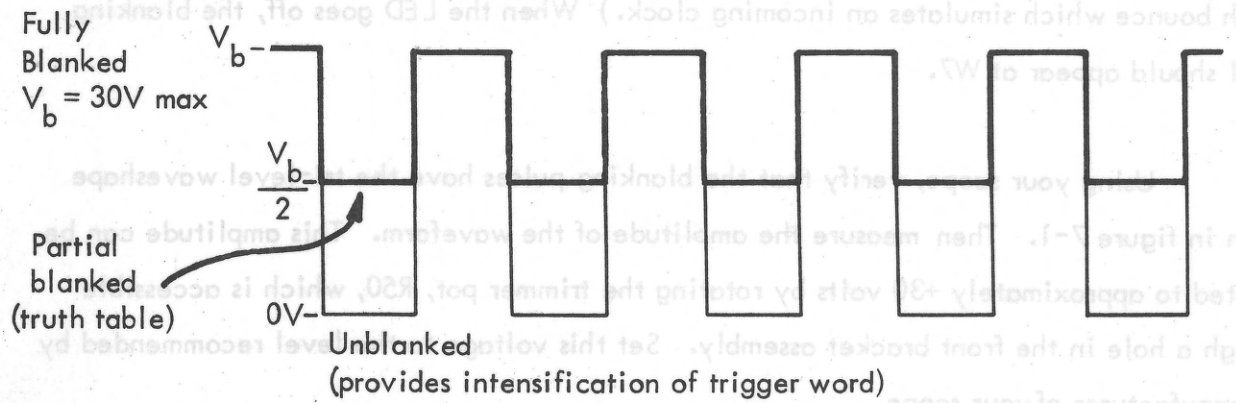
With the PC board outside of the case (IC SIDE UP), turn on AC power and verify the output of the +5 volt supply at TP1. (The locations of the test points for this section can be determined by reference to figures 6-1 or 6-2.) Then, using your scope, check for the presence of the display clock at TP3. (The clock frequency should be approximately 20 kHz.) Activate the blanking output pulse train at W7 by setting the 8 trigger switches to the "X" (center) position, selecting the SINGLE mode, pressing the RESET button to turn on the LED, and finally, flipping the clock polarity switch one or more times. (This last step generates switch bounce which simulates an incoming clock.) When the LED goes off, the blanking signal should appear at W7.

Using your scope, verify that the blanking pulses have the tri-level waveshape shown in figure 7-1. Then measure the amplitude of the waveform. This amplitude can be adjusted to approximately +30 volts by rotating the trimmer pot, R50, which is accessible through a hole in the front bracket assembly. Set this voltage to the level recommended by the manufacturer of your scope.

CAUTION

DO NOT EXCEED THE MAXIMUM BLANKING VOLTAGE RECOMMENDED BY THE MANUFACTURER OF YOUR SCOPE; OTHERWISE DAMAGE TO THE SCOPE'S BLANKING CIRCUIT MAY RESULT.

Set your scope's vertical amplifier to approximately 0.5 volts/cm and the sweep to 1 ms/cm to check the D/A signals at W5 (HOR) and W6 (VERT). They should look like the "descending staircase" waveforms of figures 7-2 and 7-3, respectively. Now set your scope for XY operation and connect the HOR, and VERT outputs to the corresponding inputs of the scope. (Do not connect the BLANK output at this time.) In order to assure a clean display, it's important to use co-axial type cable (RG-58/U) when interconnecting the analyzer and your scope; use of uncalibrated scope probes or faulty cables can severely distort the appearance of the display.



Analyzer Settings	Scope Settings
Trigger Switches = "X" Single Mode Reset Flip clock polarity switch	Vert = 5V / cm Sweep = 50 μs / cm

FIG. 7-1. Blanking output signal.

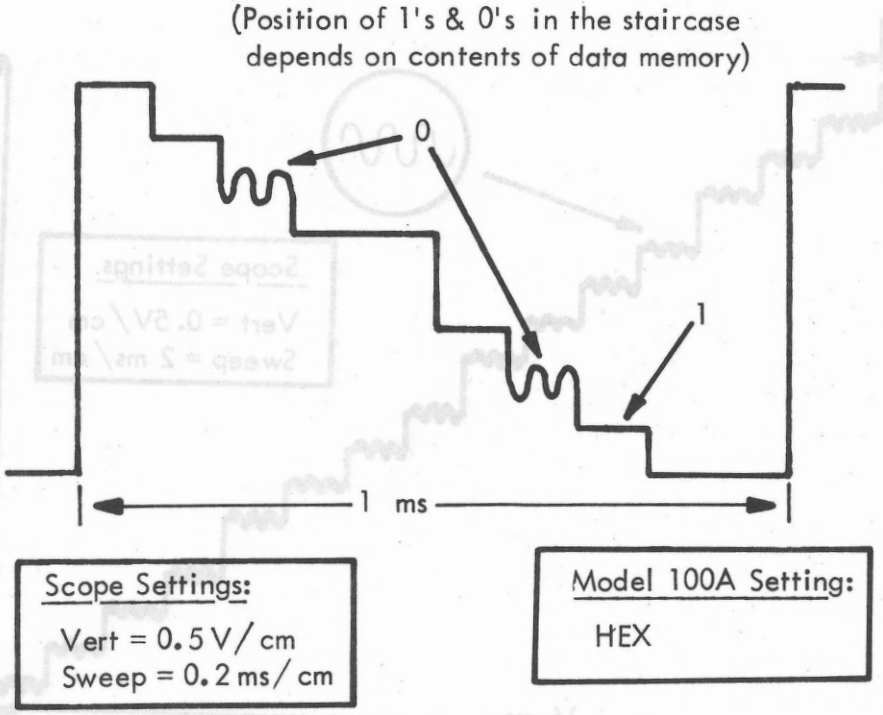


FIG. 7-2. Horizontal D/A output signal.

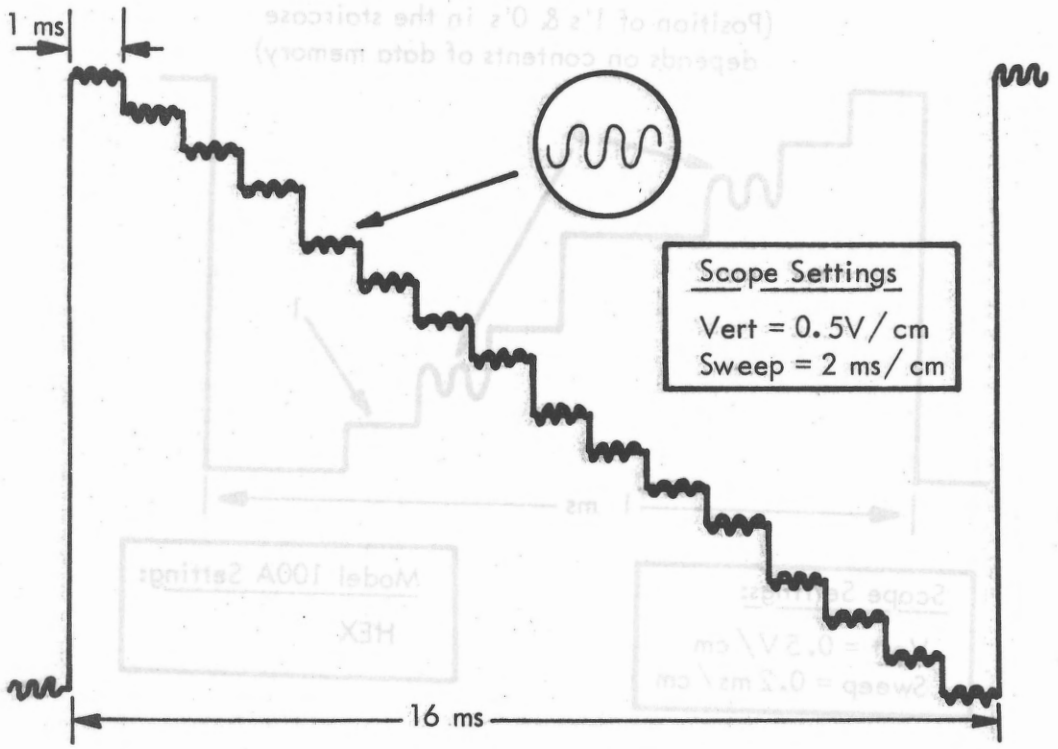


FIG. 7-3. Vertical D/A output signal.

Next set your scope's horizontal and vertical amplifiers to approximately 0.5 volts/cm. (If your scope has insufficient horizontal gain adjustment, use the maximum gain it has for the time being; later you can refer to Section 8.0 for recommendations about how to increase horizontal gain.) With the input probes unconnected and the trigger switches still set to "X," press the RESET button to illuminate the LED and again flip the clock polarity switch. When the LED turns off, the truth table should appear on the CRT. Adjust the scope's horizontal gain, vertical gain, and positioning controls until the table is centered and fills most of the screen. Then adjust the scope's focus and intensity controls to obtain a "clean" display.

With the analyzer's blanking output unconnected, faint lines between the characters in the truth table will be visible, particularly when the scope's intensity is turned all the way up. (Note however, with the intensity control properly set, the table is still quite readable.) Now connect the analyzer's blanking output to the associated input of your scope, again using co-axial cable. If the blanking voltage has been set properly, the faint lines will disappear, and the trigger word will become intensified. (You will probably have to readjust the intensity control on your scope to account for the blanking voltage.) Note that the intensified trigger word should be at the top of the truth table if the analyzer is in the positive time mode, and at the bottom if it's in the negative time mode.

One interesting feature of the Model 100A Logic Analyzer is that you can use it to observe and learn its own operation. For example, to see how the 4-bit address of the data memory sequentially changes during data collection, connect the first four input probes, BIT 0 - BIT 3, to IC8, pins 14, 13, 12 and 11, respectively. (Note that use of an IC clip would be convenient for this test.) Then using a ball clip, connect the input clock to IC2, pin 12, or TP3. Set the analyzer's controls to: HEX, REPEAT, NEG. TIME, and the clock polarity switch to the negative edge position. Next set the trigger switches corresponding to inputs D0-D3 to 1111 and the remaining trigger switches to "X." You should then see this trigger word intensified at the bottom of the table, with the 15 prior address words (1110 - 0000) listed in sequence above. Repeat this test using the upper four input probes D4-D7.

Check the trigger output by monitoring the signal at the BNC connector labeled "TRIG." It should be a high-to-low going pulse every time the trigger word occurs.

Continue to familiarize yourself with the operation of the analyzer by triggering from different address locations and changing the settings of the HEX/OCT and POS/NEG time mode switches to verify their proper operation.

If you have the opportunity, we recommend that you construct the simple CMOS dual-counter circuit of figure 7-4. Since this circuit exercises all probe inputs using one CMOS IC, it provides a convenient way of checking the operation of the Model 100A--particularly when the unit is closed up and the above self-testing mode is not readily accessible.

At this point you can go back to the previous section and follow the instructions for mounting the PC board and front bracket assembly into the case. But if you have any questions about the appearance of the display or about the proper functioning of the analyzer's circuits, go directly to Section 8.0.

IMPORTANT NOTE

Whenever connecting the Model 100A to an external circuit, it's a good idea to always attach the ground (black) probe first. This precaution will prevent damage to the input buffers in the event that the circuit under test and the analyzer do not have a common ground.

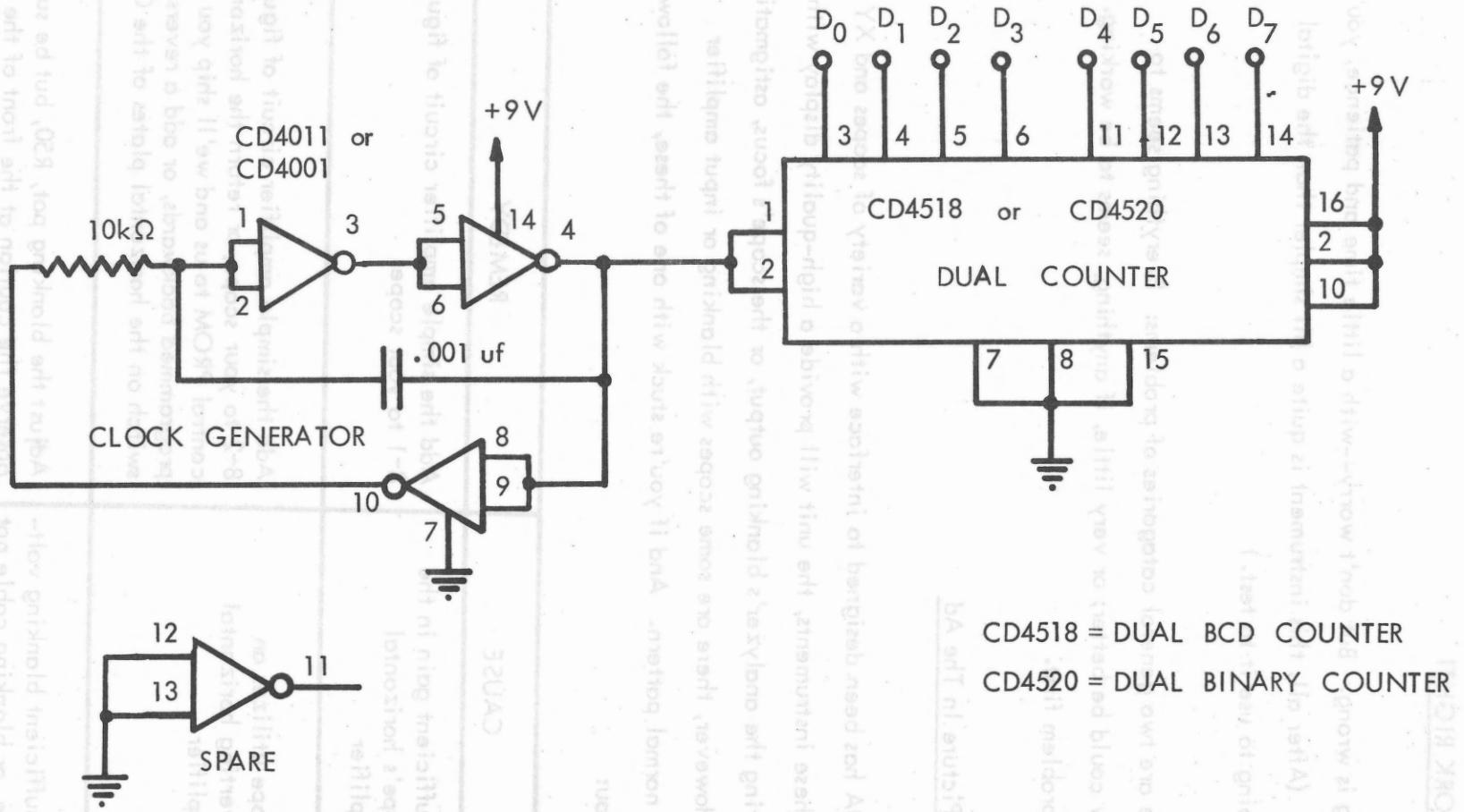


FIG. 7-4. Simple CMOS test circuit.

8.0 IT DOESN'T WORK RIGHT!

Ok. Something is wrong. But don't worry--with a little time and patience, you'll get the analyzer working. (After all, this instrument is quite a bit simpler than the digital systems you're probably going to use it to test.)

Basically, there are two general catagories of problems: Everything seems to work right, but the display could be better; or very little, if anything, seems to be working. We'll discuss the display problem first.

It Doesn't Look Like The Picture In The Ad

The Model 100A has been designed to interface with a variety of scopes and XY displays. With many of these instruments, the unit will provide a high-quality display with no more effort than adjusting the analyzer's blanking output, or the scope's focus, astigmatism and intensity controls. However, there are some scopes with blanking or input amplifier circuits that don't fit the normal pattern. And if you're stuck with one of these, the following suggestions should help you:

PROBLEM	CAUSE	REMEDY
The display is clean but it's too narrow	Insufficient gain in the scope's horizontal amplifier	Add the simple amplifier circuit of figure 8-1 to your scope.
The display is reversed.	Scope utilizes an inverting horizontal amplifier.	Add the simple amplifier circuit of figure 8-2 to your scope, or return the horizontal control PROM to us and we'll ship you one programmed backwards, or add a reversing switch on the horizontal plates of the CRT.
Faint lines between "1's" and "0's" are visible and the trigger word is not adequately intensified	Insufficient blanking voltage, or blanking cable not hooked up properly.	Adjust the blanking pot, R50, but be sure to observe the caution at the front of the manual. Also inspect cables.

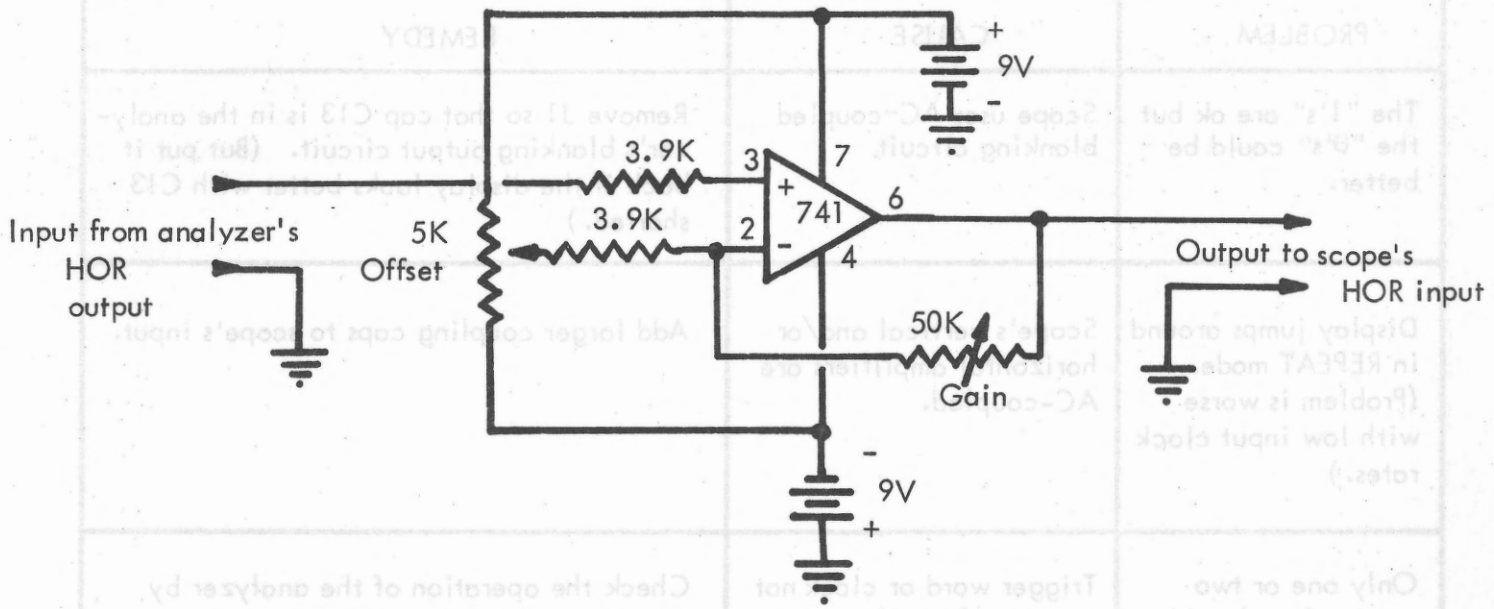


FIG. 8-1. Simple non-inverting amplifier to boost scope's horizontal gain.

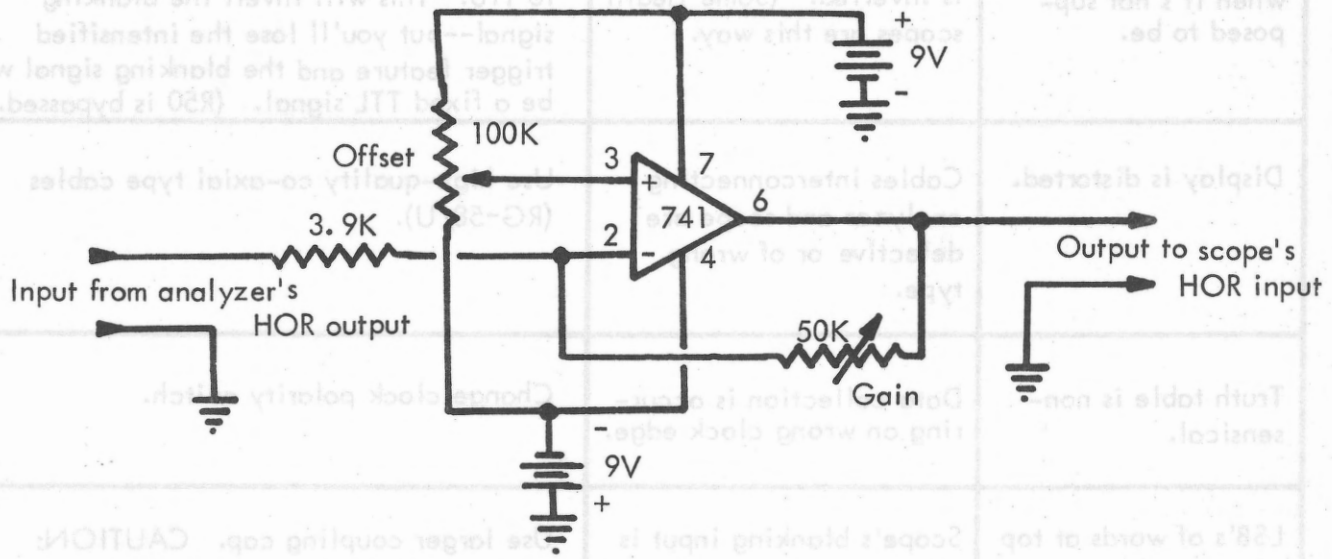


FIG. 8-2. Simple inverting amplifier to correct reversed display. Also provides gain if required.

PROBLEM	CAUSE	REMEDY
The "1's" are ok but the "0's" could be better.	Scope uses AC-coupled blanking circuit.	Remove J1 so that cap C13 is in the analyzer's blanking output circuit. (But put it back if the display looks better with C13 shorted.)
Display jumps around in REPEAT mode. (Problem is worse with low input clock rates.)	Scope's vertical and/or horizontal amplifiers are AC-coupled.	Add larger coupling caps to scope's input.
Only one or two words of truth table appear on CRT.	Trigger word or clock not present. (You'll need at least 16 clock pulses to get a display.)	Check the operation of the analyzer by setting the trigger switches to "X," and the mode switch to SINGLE. Then press RESET button and flip the clock polarity switch to generate a display.
Display is blanked when it's not supposed to be.	The scope's blanking input is inverted. (Some Heath scopes are this way.)	Remove the wire from W7 and connect it to TP6. This will invert the blanking signal--but you'll lose the intensified trigger feature and the blanking signal will be a fixed TTL signal. (R50 is bypassed.)
Display is distorted.	Cables interconnecting analyzer and scope are defective or of wrong type.	Use high-quality co-axial type cables (RG-58/U).
Truth table is nonsensical.	Data collection is occurring on wrong clock edge.	Change clock polarity switch.
LSB's of words at top of truth table are slightly lighter then other bits.	Scope's blanking input is AC-coupled.	Use larger coupling cap. CAUTION: THIS IS USUALLY A HIGH-VOLTAGE CIRCUIT: MAKE SURE ALL CAPS ARE DISCHARGED. ALSO, THE CAP INSTALLED MUST HAVE THE VOLTAGE RATING OF THE ORIGINAL.

It Doesn't Work Too Well At All

This is the situation where you wished the analyzer were working enough to even have one of the preceding display clean-up problems. The kind of problem you might be having will probably be one of the following:

1. You have a poor or missing solder joint. Go over each one carefully using your 2X magnifying glass.

2. IC's or other parts are mis-located. Check all parts for proper location and orientation against the assembly drawings of figure 6-1 and 6-2. (Take plenty of time to do this--it'll be worth it.)

3. A component has gone bad. This is unlikely, but possible. (We test all IC's and transistors prior to shipment; occasionally, however, a component will fail a short time after it's put into service.) If any component is too hot to touch, it's definitely gone bad.

4. A trace on the PC board or a wire is broken. Using figures 6-1 and the schematic in figure 8-3, check all IC's for power and ground. Then look for signal continuity in the portion of the circuit that's misbehaving.

If the general inspection described in the above steps fails to yield the cause of the problem, try the troubleshooting hints listed below.

NOTE: REMOVE BLANKING OUTPUT CONNECTION WHENEVER USING YOUR SCOPE IN THE NORMAL ANALOG MODE.

1. Check for the presence of +5 volts and +30 volts at TP4 and TP1, respectively.

2. Check for the presence of the 20 kHz clock at TP3.

3. If the display is spaced unevenly or "mixed-up" in some other way, compare the analyzer's HOR and VERT output waveforms with figures 7-2 and 7-3. If you note any major differences, make sure that all of the resistors in the ladder networks (i.e., R59, R58, R55, R49; and R45, R54, R56, R57) are of the proper tolerance and located in the correct positions on the PC board. (Note: you'll have to set the trigger switches to "X," press RESET, and flip the clock polarity switch as described previously in order to see both the horizontal and vertical D/A waveforms.)

Additional Troubleshooting Hints. (Refer to schematic in figure 8-3.)

Analyzer Never Triggers - Set all the trigger switches to "X" and provide a continuous input clock (or simulate one by flipping the clock polarity switch). Then, if the LED remains on, indicating that the unit never triggered, check the trigger bus at pin 10 of the input probe. You should see a continuous logic 1 level. If you do not, check IC3 and the connections of S1-S8. Then trace back through the two latches, IC4 and IC5, and the two input buffers IC1 and IC2. (Somewhere in this input data path, you'll probably find a stuck bit.)

If the trigger bus is O. K., then check pin 2 of the vertical counter, IC8. This is the clock input to the counter. In the non-triggered (data collection) mode, this input should be equal to the external clock. If this is not the case, check IC11, IC22, and the associated logic for proper signal levels. (In the display mode, after the unit is triggered, this same input should be equal to the internal display clock at TP3.)

Data Memory Not Collecting Properly - Check the write enable inputs at pin 3 of both RAMS (IC6 and IC7). The external clock should be present at these inputs, but only during the data collection mode. Also check the data appearing at the RAM input against the input data. This can be done simply by statically holding all 8 input data probes first to a logic 0 level, and then to a logic 1 level. (The data memory should have these same static logic levels at its inputs.)

POS/NEG Time Mode Not Operating Properly - In the positive time mode, check IC24, pin 2, for a positive-going pulse at the occurrence of the first displayed word. In the negative time mode, check IC23, pin 8, for a positive-going pulse at the occurrence of the last displayed word.

Horizontal Portion of Display Not Functioning Properly - Check the signal "HORZMSB" at IC17, pin 11. It should run continuously at a frequency of approximately 1 KHz.

Insufficient Blanking Signal - If the blanking signal cannot be adjusted to approximately 25-30 volts, check Q1 and Q2 for proper orientation.

No Blanking Signal - Check TP6 for the presence of an active low blanking signal. If it isn't present, trace back through IC23, IC18, and IC15 for the right logic levels.

If all else fails, contact your dealer for assistance. If your dealer does not have adequate repair facilities, or if you've purchased the Model 100A directly from Paratronics, Inc., then write to us describing the problem. DO NOT RETURN THE MODEL 100A WITHOUT OUR AUTHORIZATION. See Section 12.0 for complete information concerning service.

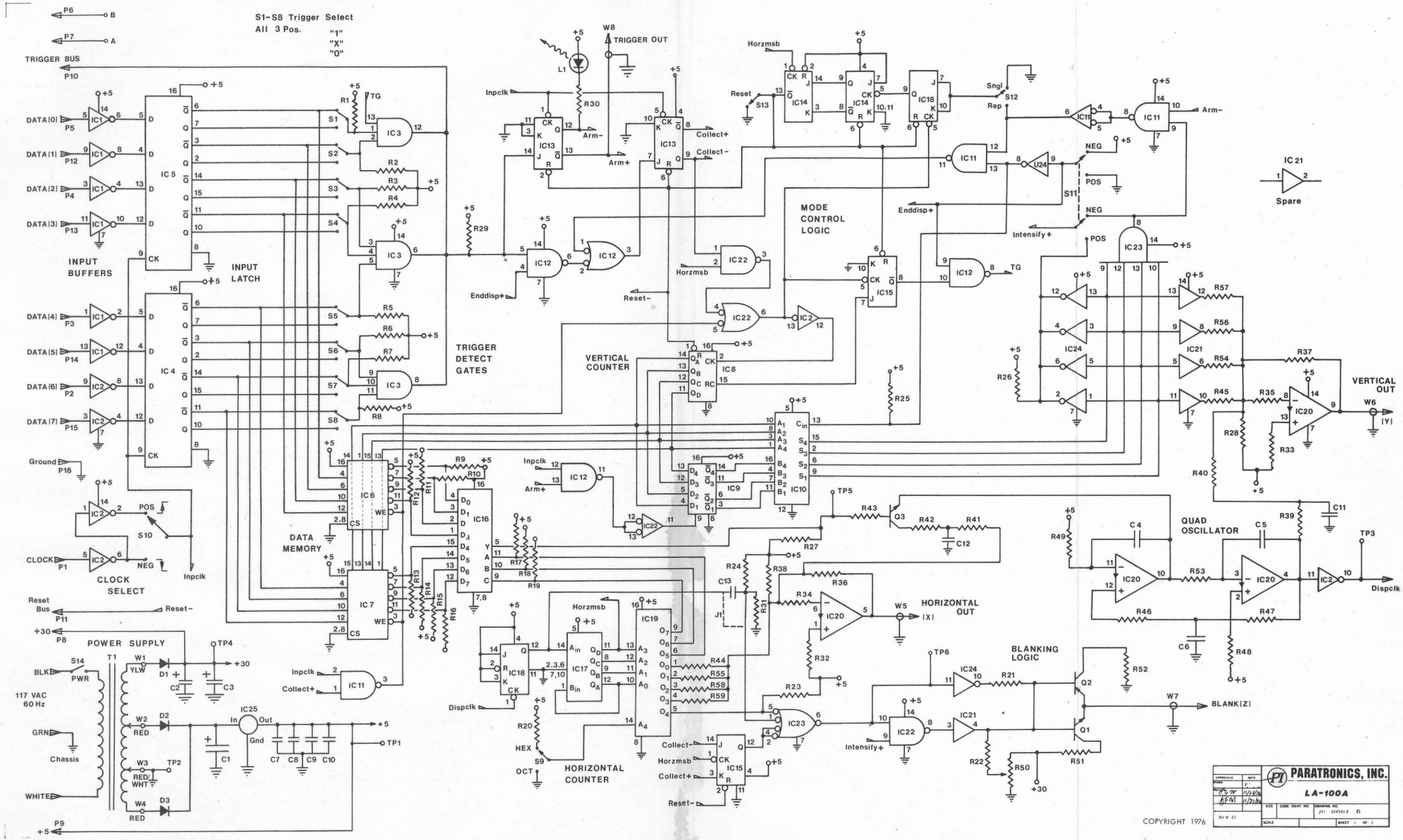
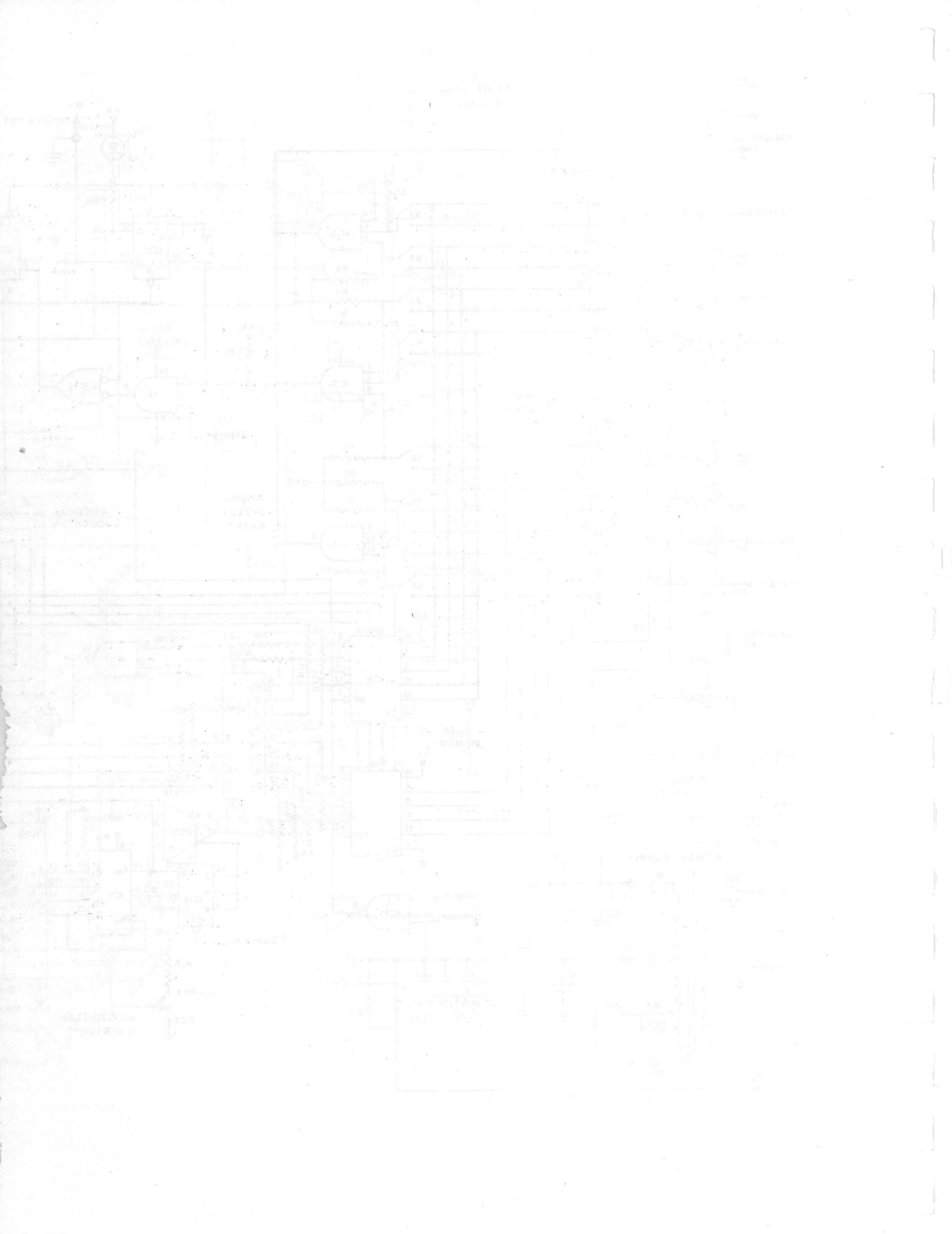


FIG. 8-3. Model 100-A Logic Analyzer Schematic.



9.0 ADDITIONAL CAPABILITIES

In this section, we'll discuss some of the built in features of the Model 100A which can expand its utility beyond what we have described thus far.

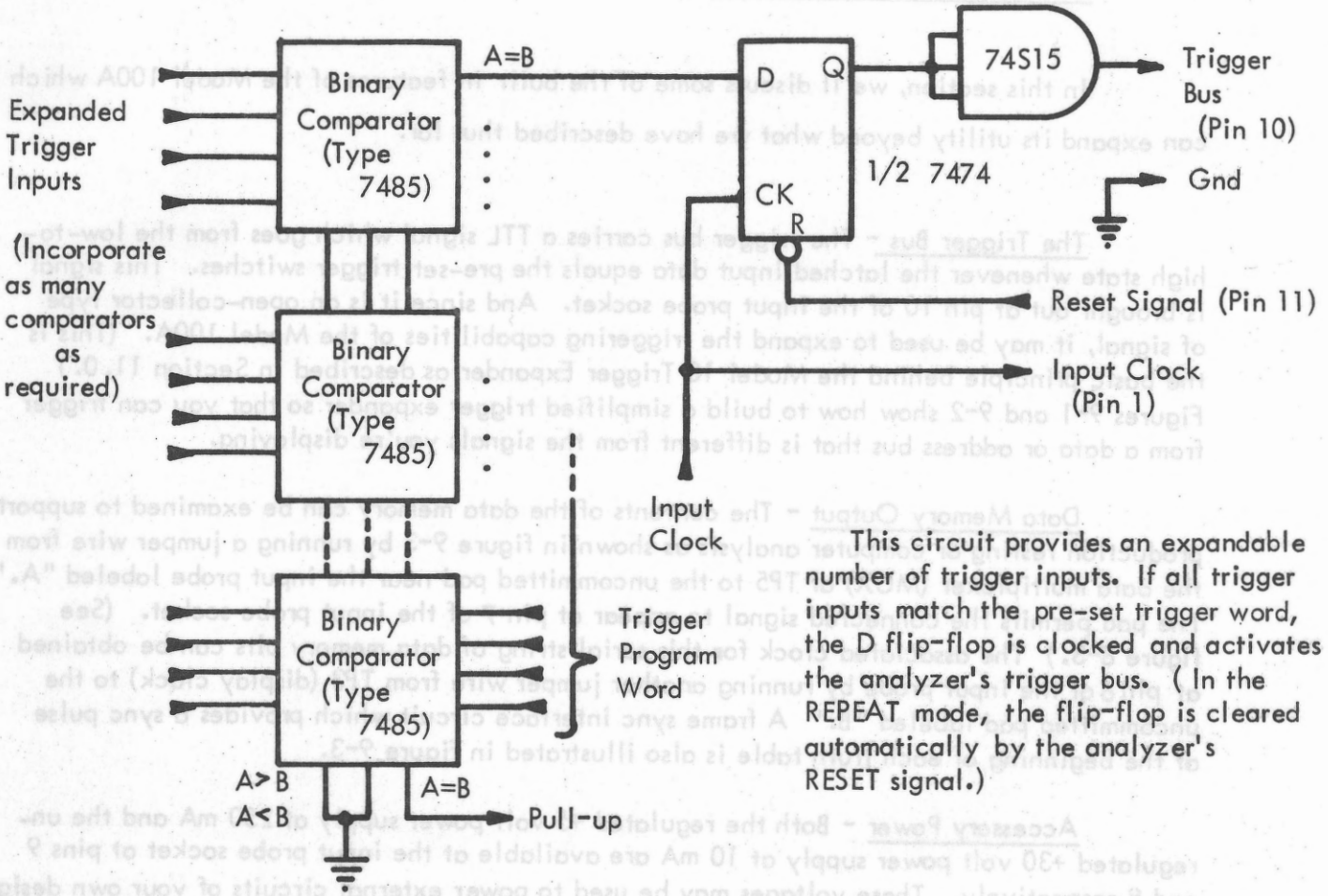
The Trigger Bus - The trigger bus carries a TTL signal which goes from the low-to-high state whenever the latched input data equals the pre-set trigger switches. This signal is brought out at pin 10 of the input probe socket. And since it is an open-collector type of signal, it may be used to expand the triggering capabilities of the Model 100A. (This is the basic principle behind the Model 10 Trigger Expander as described in Section 11.0.) Figures 9-1 and 9-2 show how to build a simplified trigger expander so that you can trigger from a data or address bus that is different from the signals you're displaying.

Data Memory Output - The contents of the data memory can be examined to support production testing or computer analysis as shown in figure 9-3 by running a jumper wire from the data multiplexer (MUX) at TP5 to the uncommitted pad near the input probe labeled "A." The pad permits the connected signal to appear at pin 7 of the input probe socket. (See figure 8-3.) The associated clock for this serial string of data memory bits can be obtained at pin 6 of the input probe by running another jumper wire from TP3 (display clock) to the uncommitted pad labeled "B." A frame sync interface circuit which provides a sync pulse at the beginning of each truth table is also illustrated in figure 9-3.

Accessory Power - Both the regulated +5 volt power supply at 250 mA and the unregulated +30 volt power supply at 10 mA are available at the input probe socket at pins 9 and 8 respectively. These voltages may be used to power external circuits of your own design as long as you don't exceed each supply's limited current handling capability.

Accessory Interconnection - Interfacing with external accessory circuits is achieved by using a 16-pin flat ribbon cable with DIP plugs on both ends.

Connecting Two or More Model 100A's - By connecting the trigger bus and the clock inputs of 2 or more analyzers together, you can expand both trigger and display capability in increments of 8 bits. For example, figure 9-4 illustrates how to connect 2 Model 100A's together so that 8 bits of the data bus and 8 bits of the address bus of a computer under test can be monitored. With this set-up, you can trigger from the data bus, the address bus, or both. You can also display either bus using a simple 3-pole, two-position switch as a multiplexer. And, if you want to see two 8-bit truth tables simultaneously, you can implement the multiplexer electronically. However, in order to do this properly, you'll have to provide an offset voltage to the horizontal D/A output of analyzer #2, so that its truth table will appear along side that of analyzer #1. The control signal which switches the multiplexer between analyzer outputs can be readily derived from the frame sync generator circuit of figure 9-3.



This circuit provides an expandable number of trigger inputs. If all trigger inputs match the pre-set trigger word, the D flip-flop is clocked and activates the analyzer's trigger bus. (In the REPEAT mode, the flip-flop is cleared automatically by the analyzer's RESET signal.)

FIG. 9-1. Model 100A trigger bus expansion.

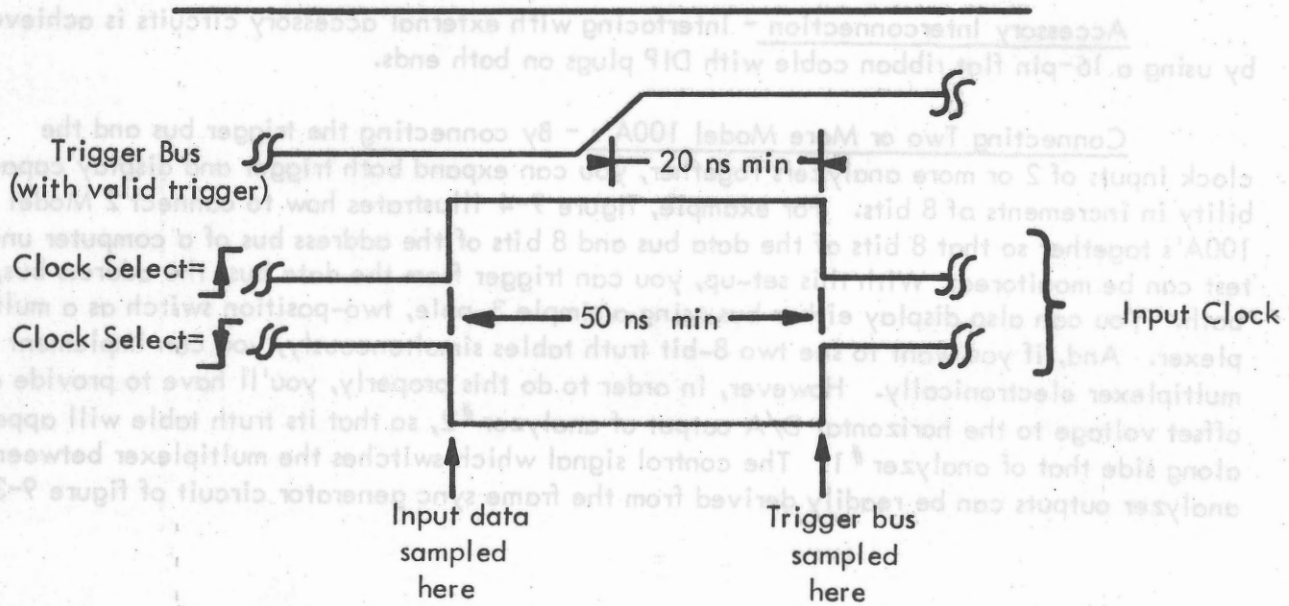


FIG. 9-2. Trigger bus expansion timing.

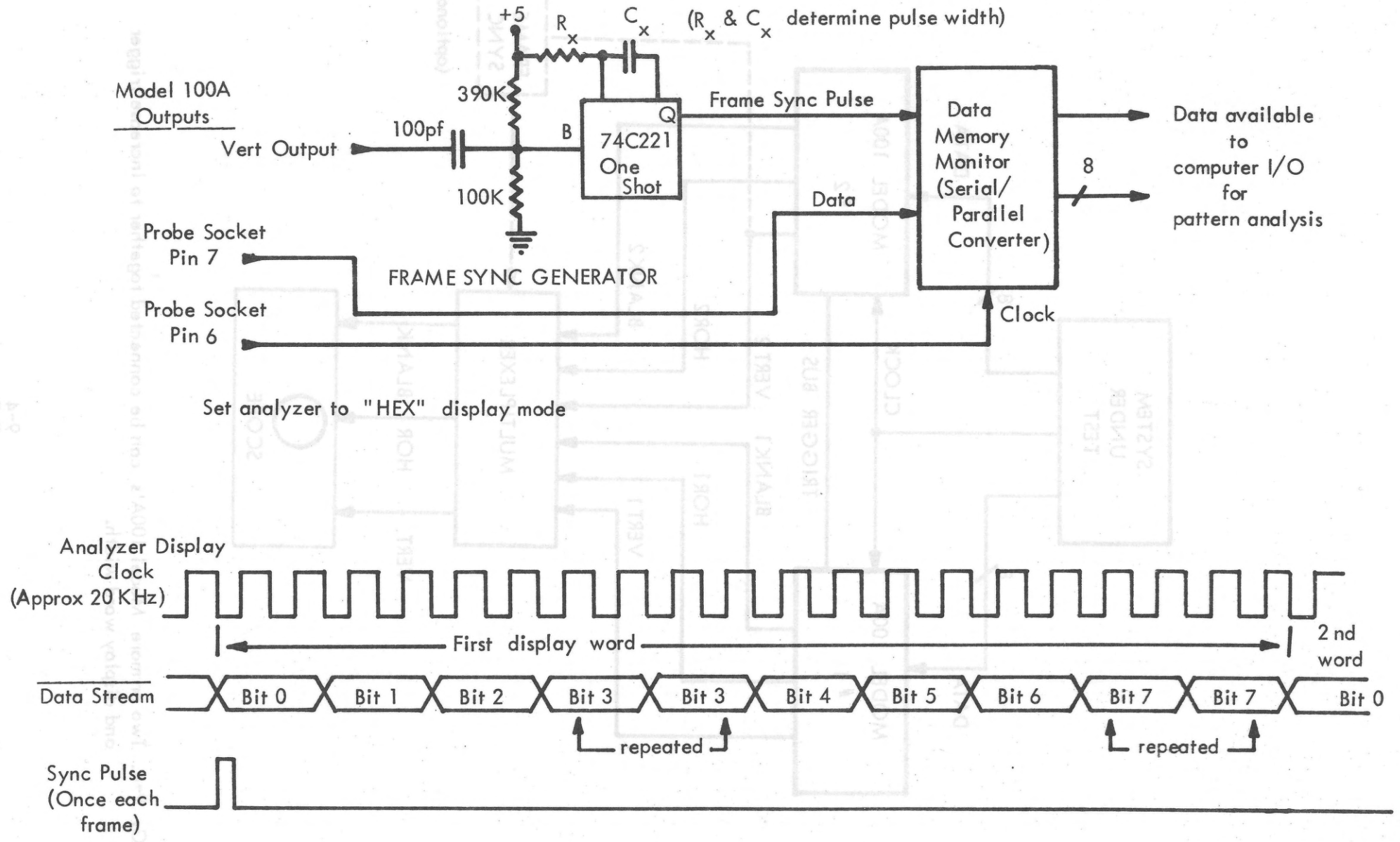


FIG. 9-3. Remote monitoring of Model 100A data memory.

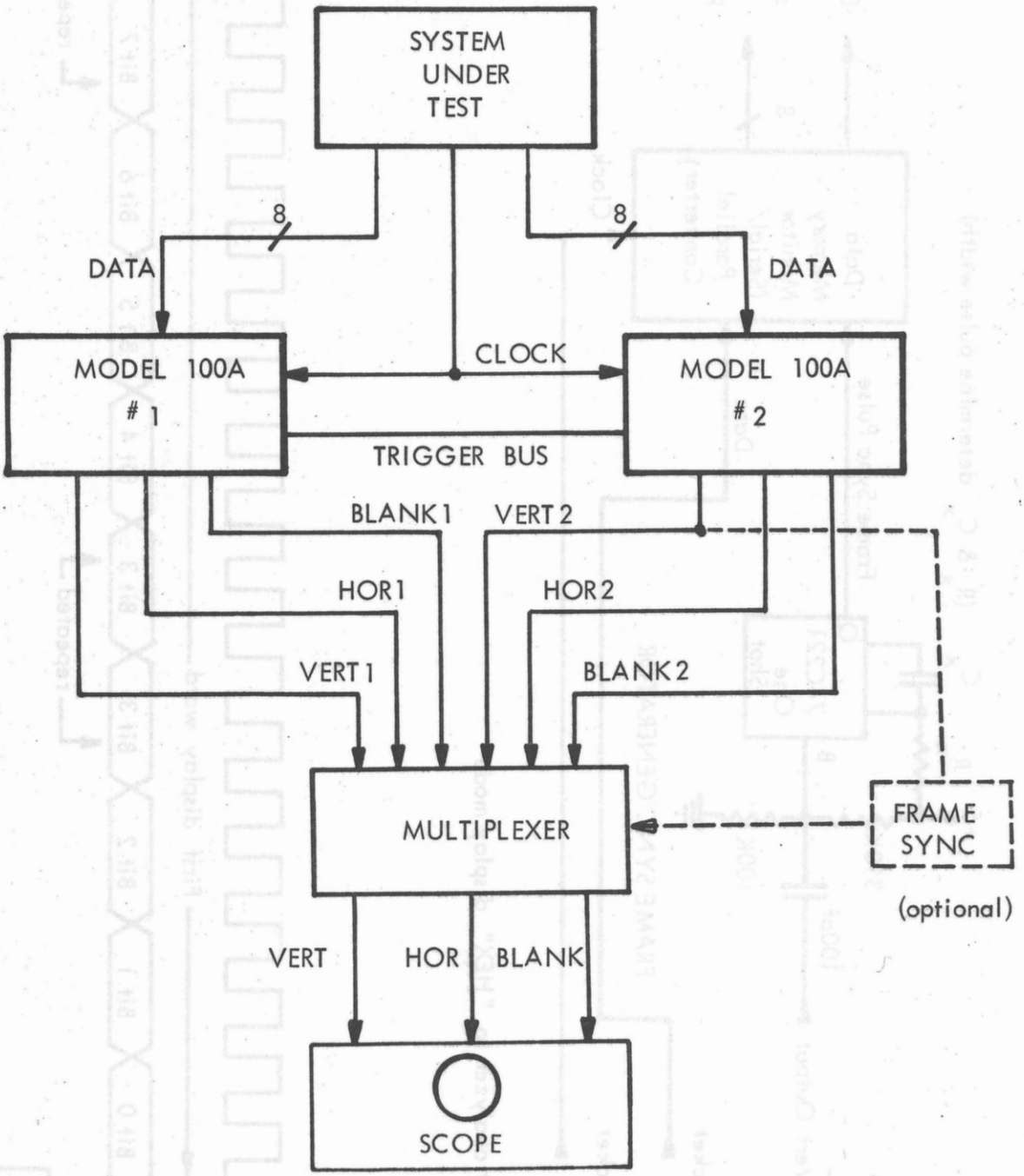


FIG. 9-4. Two or more Model 100A's can be connected together to increase trigger and display word width.

10.0 ALTAIR 8800 APPLICATION EXAMPLE

If you have an ALTAIR, the following demonstration example will show you how useful the Model 100A can be in tracing program flow in machine language.

1. Set the analyzer's controls as follows: OCT, REPEAT, negative clock edge, NEG TIME, and the trigger switches to 100 000 001. (The "1" is the LSB.)

2. Using IC clips, "E-Z" hooks, or ball clips, connect the analyzer's input probes to the ALTAIR's CPU board as follows:

   a. Clock input probe to IC J, pin 7.
   b. DØ probe to IC D, pin 12.
   c. D1 probe to IC D, pin 14.
   d. D2 probe to IC E, pin 4.
   e. D3 probe to IC E, pin 2.
   f. D4 probe to IC E, pin 14.
   g. D5 probe to IC E, pin 12.
   h. D6 probe to IC E, pin 10.
   i. D7 probe to IC E, pin 6.
   j. Ground probe to IC E, pin 8.

3. Next, run the following ADD and STORE program in the ALTAIR:

ADDRESS (OCTAL)	OCTAL CODE	MNEMONIC
400	072	LDA
401	200	(LS ADDRESS)
402	000	(MS ADDRESS)
	***	
403	107	MOV (A→B)
404	072	LDA
405	201	(LS ADDRESS)
406	000	(MS ADDRESS)
	***	
407	200	ADD (B+A)
410	062	STA
411	202	(LS ADDRESS)
412	000	(MS ADDRESS)
413	303	JMP
414	000	(LS ADDRESS)
415	001	(MS ADDRESS)

***Note: The operands read from memory will appear at these points in the displayed truth table. In this example, use 125 (octal) and 252 (octal), respectively, to observe the truth table of figure 4-2.

11.0 THE MODEL 10 TRIGGER EXPANDER

It was described in Section 9.0 how the trigger bus is available at the input probe socket. This remote triggering capability is used in the Model 10 Trigger Expander to provide a full 25-bit-wide trigger word with selectable delay. The Model 10 Trigger Expander greatly improves the flexibility of the Model 100A, especially in cases where triggering on a microprocessor's address bus, data bus, or both, is desirable.

The Model 10 plugs directly into the input probe socket and receives power from the Model 100A analyzer. It is designed so it can also be used in a stand alone mode where it provides a conditioned, delayed, trigger to other instruments such as an oscilloscope or counter. (In the stand-alone configuration it must be powered with an external 5-volt supply.)

Figure 11-1 shows the block diagram of the Model 10 and a brief functional description is given below. Figure 11-2 shows how it's connected between the Model 100A and the system under test. Further information and application notes are contained in the Model 10 Trigger Expander Assembly and Operation Manual. (The Model 10 is being prepared for production: write to us regarding its availability.)

Address Triggering - The Model 10 accepts inputs from 16 address lines. Four thumbwheel hex switches permit qualifying the trigger on a specific 16-bit address.

Trigger Qualifier - A qualifier input for the address trigger is provided and is selectable as either "1," "0," or "X," (don't care). When the Model 10 is connected to the Model 100A, there are a total of 25 trigger qualifiers: 16 address inputs + 1 qualifier + 8 data inputs.

Clock Qualifier - A clock qualifier on the Model 10 allows conditioning the clock to control the sampling and trigger detection of both the Model 10 and Model 100A. For example, by qualifying the clock on the write request signal of a microprocessor, only STORE type operations will be sampled and displayed by the Model 100A.

Trigger Delay - Three 10-digit thumbwheel switches on the Model 10 permit delaying the triggering of the Model 100A from 0 to 999 events. These events can be either clock pulses or trigger occurrences. With this useful feature, its possible to trigger the analyzer on the "nth" pass through a particular program loop, where n is between 0 and 999.

Data Multiplexing - The Model 10 also contains logic to multiplex the 8 data bits, the upper address byte, and the lower address byte. This feature makes it possible to view all 24 bits in groups of 8 by simply changing the Model 10's multiplex switch.

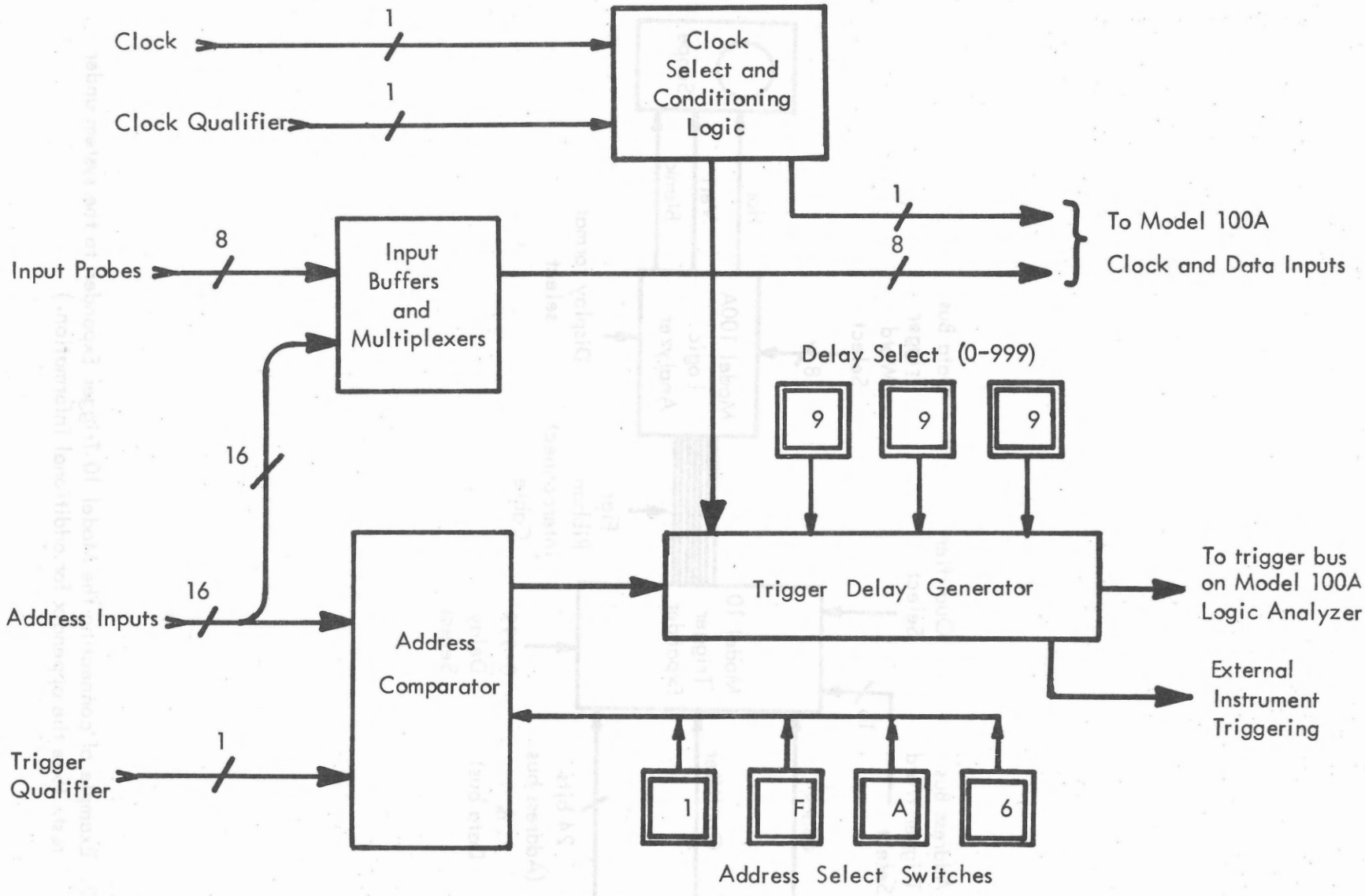


FIG. 11-1. Block diagram of the Model 10 Trigger Expander

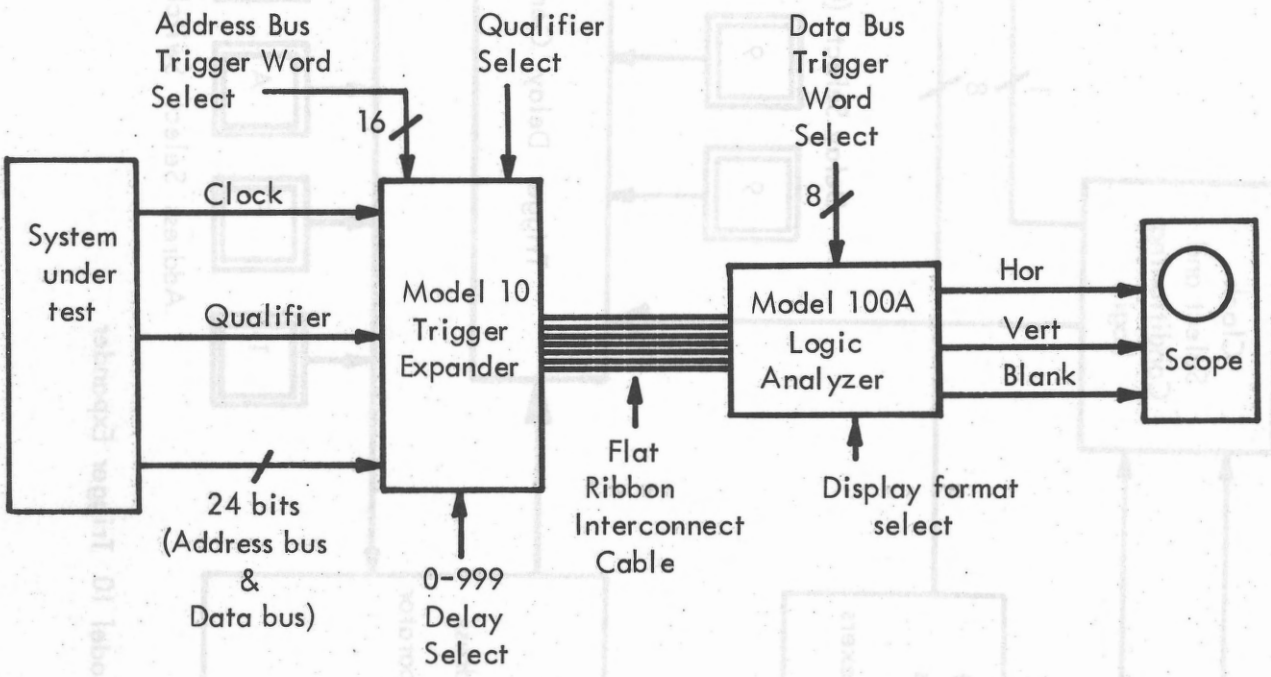


FIG. 11-2. Example of connecting the Model 10 Trigger Expander to the system under test. (See the appendix for additional information.)

12.0 THE WARRANTY AND RETURN SHIPPING INSTRUCTIONS

FULL WARRANTY

YOUR MODEL 100A LOGIC ANALYZER, purchased from Paratronics, Inc. in ASSEMBLED & TESTED form, is guaranteed against all defects in material and workmanship for a period of one (1) year from the date of shipment to the original purchaser. All factory assembled units returned to Paratronics, Inc., POST-PAID, during the one year warranty period, will be replaced or restored to proper working condition, and returned to the sender without charge.

The KIT version of the MODEL 100A LOGIC ANALYZER is guaranteed against defects in supplied parts for a period of three (3) months from date of shipment to original purchaser. Defective parts returned to Paratronics, Inc., POST-PAID, during the 3-month warranty period, will be replaced free of charge.

NOTE: THIS WARRANTY DOES NOT APPLY TO DAMAGE CAUSED BY SHIPPING, ACCIDENT, UNAUTHORIZED REPAIR, IMPROPER ASSEMBLY, ABUSE, MISUSE, OR MODIFICATION. ALSO, THIS WARRANTY IS IN LIEU OF ANY OTHER WARRANTY EXPRESSED, IMPLIED, OR STATUTORY; AND NO AGREEMENT EXTENDING OR MODIFYING IT WILL BE BINDING UPON PARATRONICS, INC., UNLESS EXECUTED BY A DULY AUTHORIZED OFFICER.

If you have a problem with the Model 100A kit or factory assembled unit, see where you fit in the categories listed below, and follow the directions given:

1. You've purchased a kit or assembled unit directly from Paratronics, Inc., and it's still covered by the warranty:

Write to Paratronics, Inc. explaining the problem in as much detail as possible. We'll promptly provide assistance and a Return Authorization Number (R. A. N.), if required. Once you receive the R. A. N., send the part or unit to us, POST-PAID, and we'll replace or repair it free of charge.

2. You've purchased an assembled unit from a dealer who assembled it himself:

Contact the dealer directly since he provides his own guarantee on units that he assembles. (If you don't get satisfaction from the dealer, write to us so we can take the appropriate action.)

3. You've purchased a kit from a dealer which is still covered by the 3-month warranty:

Contact the dealer first since he may have the required replacement parts on hand. If not, follow the procedure in no. 1 above.

4. You've purchased a kit or assembled unit from Paratronics, Inc. and the warranty has expired:

Follow the procedure in no. 1 above. However, when you return the unit to us, POSTPAID, enclose $25.00 to cover repair costs. If the problem is relatively simple, we'll refund the unused portion of your remittance. On the other hand, if the problem requires extensive repair, we'll provide you with an estimate on the total cost and await your authorization before proceeding.

5. You've purchased a kit or assembled unit from a dealer and the warranty has expired:

Contact the dealer first since he may be able to provide you with fast service. However, if he is unable to provide the required service, follow the procedures in nos. 1 and 4, above.

6. Your particular situation is not covered by the above:

Write to us and tell us all about it. We'll do everything we can to help.

SHIPPING INSTRUCTIONS

1. Pack the unit or component carefully. Use plenty of foam or other cushioning material and high quality shipping tape. When shipping a complete unit, use the original container, if available, and pay particular attention to protecting the front panel controls and the finish on the case. SUGGESTION: Since most of the circuitry is contained on the printed circuit board, you may find it convenient and less costly to ship only the PC board and front bracket assembly.

2. DO NOT RETURN ANYTHING WITHOUT A RETURN AUTHORIZATION NUMBER (R.A.N.).

3. Ship the unit or component, POSTPAID, to: Paratronics, Inc., 150 Tait Avenue, Los Gatos, CA. 95030.

4. For your own protection, we recommend that you insure the shipment against loss or damages.

APPENDIX

MICROCOMPUTERS & OTHER APPLICATIONS

A.1 GENERAL DIGITAL APPLICATIONS

In this first section, we'll provide you with some guidance in using the Model 100A Logic Analyzer to view the operation of simple digital circuits. We'll start by summarizing some of the information provided in prior sections of this manual which will enable you to correctly connect the Model 100A to your system. Then we'll discuss a simple troubleshooting example which you can extend to your own applications.

Connecting The Model 100A - First connect the analyzer's HOR, VERT, and BLANK outputs to the corresponding inputs of your scope (which should be set up for an X-Y type of display). Next, connect the black ground probe and the white clock probe to the corresponding points of the system under test. (Be sure you know whether the data in your system are valid on the positive or negative clock edge; otherwise the display may not make any sense.) Then connect the 8 data input probes (D0-D7) to those signals in your circuit you wish to monitor. Finally, set up the trigger word and display modes (HEX or OCTAL, SINGLE or REPEAT, and POS or NEG time)... and you're ready to go.

Optimum Use of the 8 Data Probes - If your circuit is fairly simple--e.g., a 4-bit counter--then the 8 data probes will allow you to look at just about all of the available input and output signals. However, if your circuit is more complex--e.g., a microprocessor--then you'll have to use the information provided later in this appendix (and good judgement) in selecting those 8 monitoring points that give you the required visibility. If you find that it would be convenient to monitor more than 8 data points, there are several things you can do:

1. Use some of the input probes to provide the desired trigger. Then move the remaining probes to different points of the circuit and take successive "readings," much in the same way you would use a voltmeter or scope probe in an analog circuit.

2. Construct a simple 9-pole, 3-position switch as shown in figure A.1-1. Then switch between the address bus, data bus, or control signal as required. (You may want to build a permanent test fixture into your computer for this purpose.)

3. Perform some pre-conditioning of selected signals to reduce the number of probe connections. The way to do this is to use external AND gates, decoders, comparators, etc.

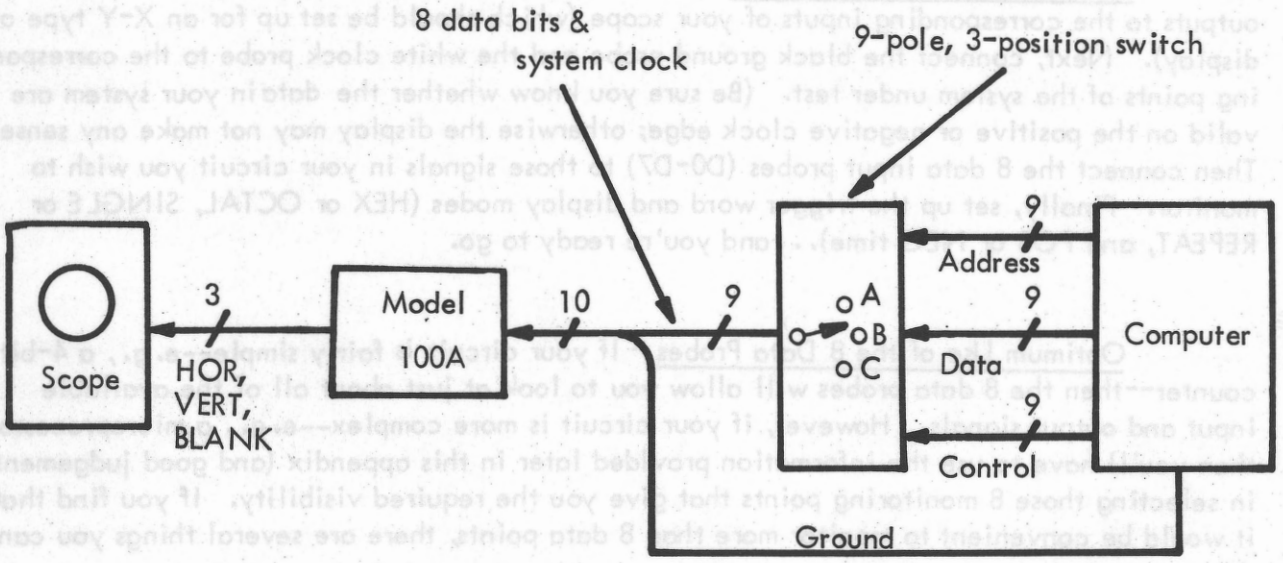


FIG. A.1-1. Multiplexing the input probe for 24-bit data monitoring.

Miscellaneous Application Hints

1. When connecting the clock and data probes, remember that the input voltage must be limited to the range of -0.5 volts to +15 volts with respect to ground. (If you don't, you might have to replace the 74LS14 input buffers--that's why they're in sockets.) Also, each probe input has an input load of 360 μA and a logic threshold of approximately 1.6 volts; so these inputs are fully compatible with most logic families: TTL, low power and regular Schottky, DTL, RTL, CMOS, N-Channel MOS, and P-Channel MOS.

2. Always connect the analyzer's clock probe to a signal in your circuit which is synchronous with the data being monitored. This is normally the system clock which clocks the flip flops, registers, counters, etc. However, other signals can be used if it's desirable to conditionally clock the data into the analyzer. For example, if you're interested in collecting data only when a particular register is updated, you can use the LOAD control of that register as the input clock.

3. With regard to the signal you use as the input clock, always obey the following rules to avoid a "garbage" display:

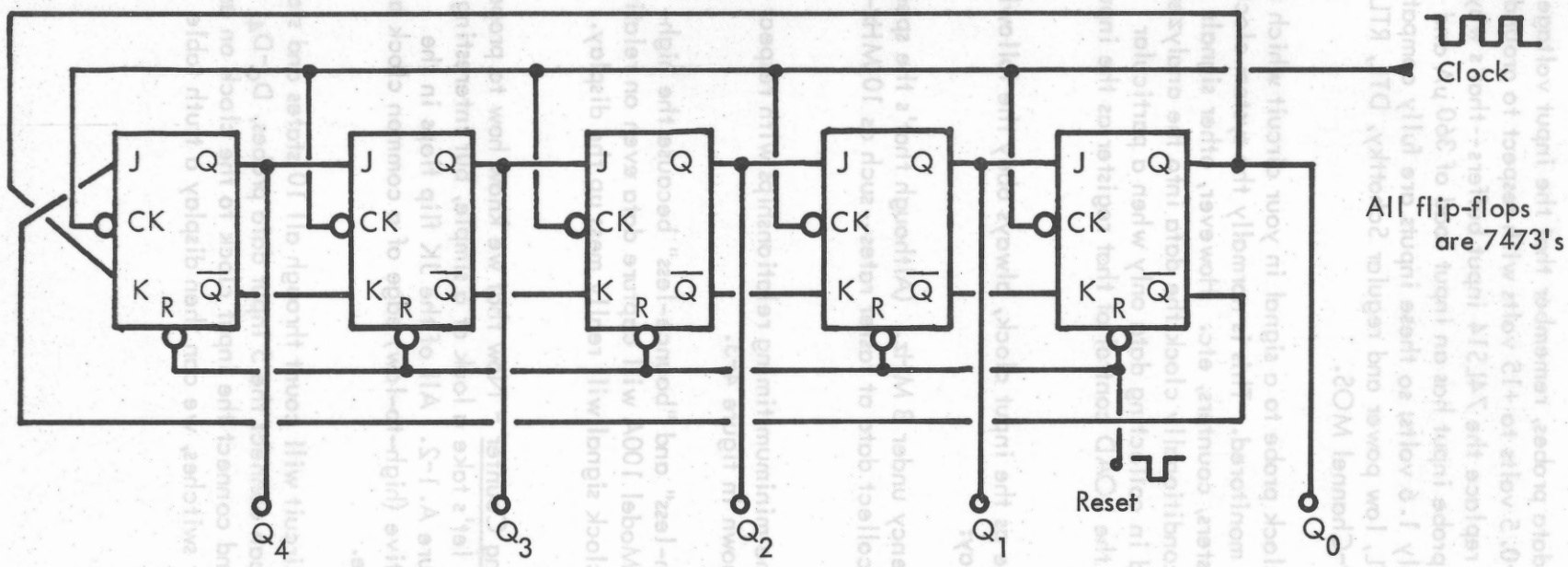
   a. Keep the input clock frequency under 8 MHz. (Although that's the spec, you'll probably be able to collect data at faster rates--such as 10 MHz--but it's risky.)

   b. The input data must have the minimum timing relationships with respect to the active clock edge as shown in figure 4-3.

   c. The clock should be "glitch-less" and "bounce-less" because the high-speed input circuits of the Model 100A will capture data even on relatively narrow spikes: a noisy clock signal will really mess up the display.

Analyzing a Faulty 5-Bit Twisted Ring Counter - Now that we know how to properly connect the Model 100A to the digital world, let's take a look at a simple, but interesting circuit: The 5-bit twisted ring counter of figure A.1-2. All of the JK flip flops in the figure are synchronously clocked on the negative (high-to-low) edge of a common clock and will count in the sequence shown in the figure.

When it's operating correctly, this circuit will count through all 10 states and start all over again. In order to observe this, we can connect the 5 input data probes, D_0-D_4, to the corresponding counter outputs, Q_0-Q_4, and connect the input clock to the clock on any one of the JK flip flops. By using the trigger switches, we can then display a truth table beginning at any state we desire.



	Q_4	Q_3	Q_2	Q_1	Q_0
Initial condition after reset	0	0	0	0	0
Condition after first clock	1	0	0	0	0
2nd	1	1	0	0	0
3rd	1	1	1	0	0
4th	1	1	1	1	0
5th	1	1	1	1	1
6th	0	1	1	1	1
7th	0	0	1	1	1
8th	0	0	0	1	1
9th	0	0	0	0	1
10th	0	0	0	0	0
etc.					

FIG. A.1-2. Five bit twisted ring counter.

Thus far, everything is cool. But let's say, while we were in the REPEAT mode, the scope's display went blank and the TRIG IND LED came on continously. This would mean that the analyzer is waiting for a trigger--but none occurred. In order to determine what the counter was doing, we would progressively move the trigger switches to the "X" (don't care) position until we observed a full truth table on the CRT. What we might see is as follows:

Q4	Q3	Q2	Q1	Q0
1	0	1	0	1
0	1	0	1	0
1	0	1	0	1
0	1	0	1	0

Etc.

It's obvious that the counter is no longer cycling through the 10 states of figure A. 1-2; it's merely oscillating through 2 illegal states. (It's interesting to note that this sequence can indeed occur with this type of circuit--even without a permanent failure of any of the JK flip flops.)

Now, let's use the analyzer to determine how this condition was erroneously entered. First, we set the trigger switches to one of the illegal states, say "10101." Then we set the analyzer to the SINGLE mode and NEG TIME. Next we apply a negative-going reset signal to the circuit as shown in figure A. 1-2. (This will permit the counter to go back into its normal 10-state sequence.) Finally, we arm the analyzer by pushing the RESET switch and we wait for the illegal state to occur. When the counter again fails and "jumps state," the analyzer will automatically trigger and, since it's in the negative time mode, it will display 15 steps leading up to that illegal state. This will tell you when the problem occurred and even which flip flop was misbehaving at that time. Can you imagine trying to get this kind of troubleshooting assistance from an oscilloscope or logic probe?

This example illustrates how the Model 100A can be used to detect abnormal or unusual circuit behavior and then trigger on an illegal logic state to rapidly identify even subtle problems. This is a new, powerful, concept in troubleshooting which is becoming essential for today's digital systems. As you gain more experience in using the Model 100A, you'll be able to analyze the operation of even the most involved digital circuits in ways that were not possible before.

A.2 MICROCOMPUTER APPLICATIONS

General Application Information

Today, the most exciting "component" of digital systems is the microprocessor. These low-cost, yet powerful, devices have permitted the use of microcomputers in applications and business areas that were not economically possible until now. Unfortunately, microcomputers require at least an order of magnitude more attention to debugging and troubleshooting then ordinary digital electronics. The Model 100A Logic Analyzer permits you to readily accomplish these troubleshooting tasks and provides a valuable tool for understanding just how and why microcomputers work--or don't work.

In this section, we'll present general applications information for using the Model 100A with microprocessors and then we'll provide a number of examples illustrating how to connect the analyzer to popular microcomputers. We'll also discuss how the Model 10 Trigger Expander Accessory can be used to enhance the capabilities of the Model 100A.

Microprocessors contain a large number of input and output logic signals. These signals take the form of address, data, control signals and clocks. As we have seen, the Model 100A permits the simultaneous viewing of any combination of up to 8 parallel signals. Of these signals, one of the most useful is the data bus of the microprocessor. This bus permits tracing both data and instructions as they flow between the memory and the microprocessor. The light input loading of the Model 100A allows it to be connected directly to most MOS microprocessor I/O data pins. (However, in a system which has a buffered I/O bus, there is less chance of affecting high-speed circuit operation by connecting the Model 100A to the buffered side of the bus.) The clock of the analyzer should be connected either to the correct phase of the system clock or to a signal whose active edge indicates the occurrence of a valid data transfer. The correct signal or clock phase can be determined by reviewing the manufacturer's specification sheet. (The required interconnection information for most popular microprocessors is also provided in the following sections.)

Another useful monitoring point is the microcomputer's address bus. This bus will provide a truth table display of memory address sequences. The use of the analyzer in the negative time mode is particularly useful for tracing the conditions leading up to the reference of a specific memory location--e.g., during a branch address.

The 8 parallel inputs of the Model 100A permit the direct monitoring of 256 addresses. While this is sufficient in many applications, there are ways of using the 8 data inputs to look at larger address spaces. The simplest of these is to use the normal decoding or chip-select circuitry of the memory to perform decoding of upper address bits. Simply connect the MS B of the input probe, D7, to the chip-select of the address space to be monitored and select the correct logic state on the trigger switch. The remaining 7 data inputs may now be used to monitor other address bits or data bits as desired. But if the required trigger word can be described in even fewer bits, the remaining inputs can be moved (i.e., multiplexed) to view additional signals. (This approach is most useful when using the REPEAT mode of the Model 100A.)

Another way to expand the triggering capability is to use one or more digital comparators tied to the trigger expander input of the Model 100A input probe socket as described in Section 9.0, figure 9-1. And as was mentioned in Section 11.0, the Model 10 Trigger Expander uses this capability to expand the trigger to 25 bits and permits delayed triggering of the analyzer.

The other useful monitoring points in microcomputers which lend themselves well to logic analysis by the Model 100A include read/write control lines, interrupt request signals, reset signals, bus enable signals and halt and wait request signals. These signals indicate correct operation of the microprocessor with other subsystems such as the control panel, memory, I/O and interrupt subsystems. One typical use of such signals would be to use a reset signal to trigger the Model 100A in the positive time mode. The remaining data inputs could then be used to verify correct start-up sequencing by monitoring memory read/write signals and/or addresses.

A.2.1 LOGIC ANALYSIS OF THE INTEL 8080

The INTEL 8080 (8080A) microprocessor is fabricated using NMOS technology and operates from +12, +5 and -5 volt power supplies. It utilizes an 8-bit, bidirectional, 3-state data bus and a separate 16-bit, 3-state address bus for addressing up to 65K bytes of memory.

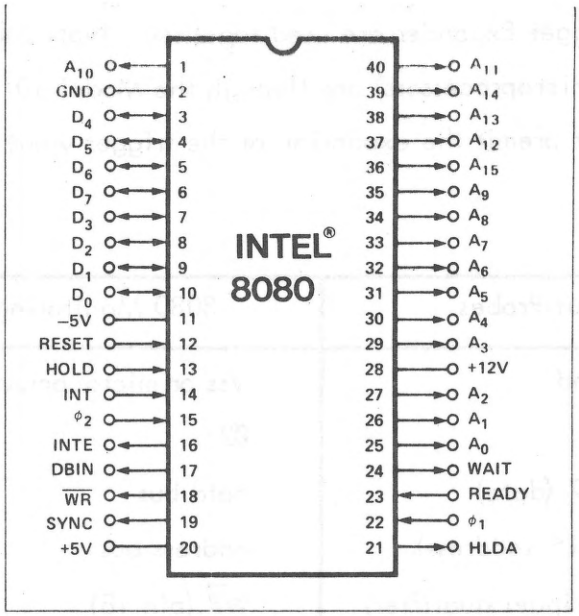
The 8080 requires 2 clock input phases (Ø1, and Ø2) and 4 control inputs. The chip provides 6 timing and control outputs to other subsystems associated with the microcomputer. Each 8080 bus is TTL-compatible and may be monitored directly by the Model 100A. (However, as was mentioned previously, use buffered address and data signals, if available.)

The pin assignments and functions of the 8080 are shown in figure A.2.1-1 for your reference.

The following two tables provide the connections and control settings required to analyze the 8080. As you became familiar with the functions of the 8080 and its supporting subsystems, move the probes to different points in the system and experiment with the various data collection and display modes of the analyzer.

Model 100A Input Probes	8080 Monitoring Points
Ground	Vss or Microcomputer ground
Clock	Ø2
D0-D7	data bus, address bus or control signals

Model 100A Control Settings	
Clock edge	positive-going
HEX/OCTAL	use OCTAL for address and data
POS/NEG TIME	As required
SINGLE/REPEAT	As required
Trigger Switches	As required



Signal Description

A_{15}-A_0	Address to memory or I/O device number for up to 256 input and 256 output devices. A_0 is LSB.
D_7-D_0	Bidirectional communication between memory, CPU, and I/O devices.
Sync	Signal to indicate the beginning of each machine cycle.
DBIN	Data Bus In signal indicates to external circuits that data bus is in input mode. (Enables the gating of data from I/O or memory onto data bus.)
READY	Valid memory or input data available on data bus. Used to synchronize 8080 with slower memory or I/O devices.
WAIT	Acknowledges that 8080 is in a wait state.
$\overline{WR}$	The write signal used for memory write or I/O output
HOLD	Requests 8080 to enter the HOLD state.
HLDA	The HOLD ACKNOWLEDGE signal responds to HOLD and indicates that address and data buses will go to high impedance state.
INTE	Interrupt Enable signal indicates content of internal interrupt enable flip-flop. Inhibits interrupt when flip-flop is reset.
INT	Interrupt request is recognized at end of current instruction or while halted.
RESET	While activated, the program counter is reset, program will start at 0 in memory. INTE and HLDA are reset.
Φ1, Φ2	External clocks; non-TTL compatible.

FIG. A.2.1-1. Intel 8080 (8080A) pin assignments and signal description.

The next two tables illustrate the connections and control settings when the Model 100A and the Model 10 Trigger Expander are used together. Note that all interconnections to the 8080 (and all other microprocessors) are through the Model 10. Also note that the two units operating together premit the expansion of the trigger word to 25 bits.

Model 10 Input Probes	8080 Monitoring Points
Ground	Vss or microcomputer ground
Clock	Ø2
D0-D7 (data)	data bus
A0-A15 (address)	address bus
Q_0 (trigger qualifier)	$\overline{WR}$ (pin 18)

Model 10 and Model 100A Control Settings	
Model 10	
Display multiplexer	data, upper address byte, lower address byte
Clock edge	positive-going
Q_0 (trigger qualifier)	"0" for write qualify; "1" for read
Q_2 (clock qualifier)	off
Delay select	clock or trigger delay
Delay set	0-999, as required
Address set	4-digit hex address, as required
Address trigger mode	off or synchronous, as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	Octal
SINGLE/REPEAT	as required
POS/NEG Time	as required
Trigger Switches	as required

With the above set-up, a 16-bit address can be pre-set to initiate triggering: at which point the display will show all of the associated program steps on the data bus.

Note that the Model 10 has the additional capability, through the use of internal multiplexers, to permit the display of the data bus, the upper byte of the memory address, and the lower byte. Also, the ability of the user to select the write request ($\overline{WR}$) line as a trigger qualifier, provides the useful feature of triggering the analyzer only when the contents of a memory location or I/O address is being modified.

Using the delay feature of the Model 10, triggering can be delayed for a pre-set number of clock cycles or trigger occurrences. This feature is useful for paging through your program or for capturing the "nth" time a particular memory reference is made.

A.2.2 LOGIC ANALYSIS OF THE MOTOROLA 6800

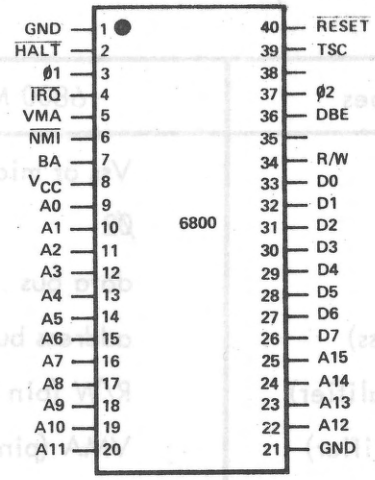
The MOTOROLA 6800 microprocessor is fabricated using NMOS technology and operates from a single +5 volt power supply. It utilizes a three-state 16-bit address bus for addressing up to 65K bytes of memory or I/O devices, and it operates with a bidirectional, three-state 8-bit data bus. The maximum clock rate is 1 MHz. All 6800 signals are compatible with the 100A logic analyzer inputs; however it's good practice to interface with the buffered side of the data bus and address bus whenever possible. Figure A.2.2-1 illustrates the 6800's pin assignments and signal descriptions.

The following tables provide the connections and control settings of the Model 100A required to analyze the 6800 microprocessor.

Model 100A Input Probes	6800 Monitoring Points
Ground	Vss or microprocessor ground
Clock	Ø2
D0-D7	data bus, address bus or control signals

Model 100A Control Settings	
Clock edge	positive-going
HEX/OCTAL	HEX
POS/NEG TIME	as required
SINGLE/REPEAT	as required
Trigger switches	as required

With the above set-up, the Model 100A will monitor all 6800 bus activity and display data bus "traffic" to and from the microprocessor and its subsystems.



Signal Description

HALT	CPU halted
IRQ	Interrupt request pending
VMA	Address bus data is valid
NMI	Non-maskable interrupt
BA	Address bus is available, CPU in wait state
RESET	Initialize CPU
TSC	Address bus and R/W line at high-impedance
DBE	Data bus drivers are enabled
R/W	Read operation into CPU, otherwise Write operation

FIG. A.2.2-1. Motorola 6800 microprocessor pin assignments and control signal descriptions.

The next two tables describe the connections and control settings required when the Model 100A is used with the Model 10 Trigger Expander. This permits expanding the trigger word to 25 bits and selectively delaying the triggering of the Model 100A. All connections to the 6800 microprocessor system are made through the Model 10.

Model 10 Input Probes	6800 Monitoring Points
Ground	Vss or microcomputer ground
Clock	Ø2
D0-D7 (data)	data bus
A0-A15 (address)	address bus
Q_0 (trigger qualifier)	R/W (pin 34)
Q_1 (clock qualifier)	VMA (pin 5)

Model 10 and Model 100A Control Settings	
Model 10	
Display multiplexer	data, upper address byte, lower address byte
Clock edge	positive-going
Q_0 (trigger qualifier)	"0" for write qualifier; "1" for read
Q_1 (clock qualifier)	"1"
Delay select	clock or trigger delay
Delay set	0-999, as required
Address set	4-digit HEX address, as required
Address trigger mode	off or synchronous, as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	HEX
SINGLE/REPEAT	as required
POS/NEG TIME	as required
Trigger Switches	as required

With the above configuration, the Model 100A can be triggered by the 6800's reference to a specific address. Also, qualifying the analyzer clock on the VMA signal allows the analyzer to sample 6800-directed bus activity only. And by setting the trigger qualifier to "0," the analyzer will trigger only on a write operation. Finally, triggering can be delayed up to 999 clock pulses or trigger occurrences by setting the appropriate delay mode into the Model 10. This feature is useful in the analysis of 6800 program loops.

A.2.3 LOGIC ANALYSIS OF THE FAIRCHILD F8 MICROPROCESSOR

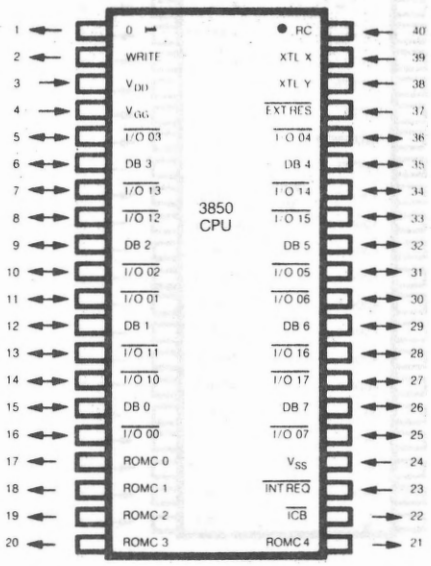
The F8 microprocessor system consists of a two-chip set which is capable of many basic processing tasks. For more complex functions, memory access and interface chips are added to the chip set. The F8 system is unique in that each chip has its own resident program counter, thus eliminating the need for a dedicated address bus. Branch operations which necessitate updating the internal address counters are multiplexed onto the data bus.

The pin assignments and signal descriptions for the 3850 F8 CPU chip are shown in figure A.2.3-1. Figure A.2.3-2 illustrates the same information for the 3853 Memory Interface Chip. The Model 100A Logic Analyzer readily permits the analysis of all F8 CPU data bus transfers and I/O operations.

The following tables provide the required information for using the Model 100A with the F8 microprocessor system:

Model 100A Input Probes	F8 Monitoring Points
Ground	Vss or microprocessor ground
Clock	Write (pin 2 of 3850)
D0-D7 inputs	DBØ-DB7

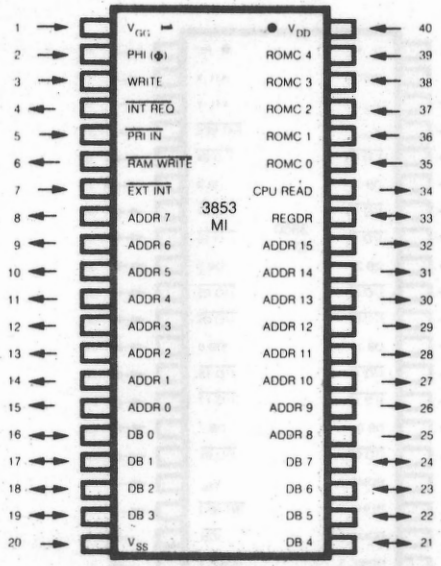
Model 100A Control Settings	
Clock edge	negative-going
HEX/OCTAL	HEX
POS/NEG TIME	as required
SINGLE/REPEAT	as required
Trigger Switches	as required



Signal Description

DB0-DB7	Bidirectional data bus
I/O 00-I/O 07	I/O Port zero
I/O 10-I/O 17	I/O Port one
ROMC 0-ROMC 4	Output control lines
RC	RC timing input
XTL-X	Crystal clock inputs
XTL-Y	External clock inputs
EXT RES	External reset
Φ, WRITE	Output clocks
ICB	Interrupt control bit
INT REQ	Interrupt request
V_{dd}, V_{ss}, V_{gg}	Power

FIG. A.2.3-1. Fairchild F8 microprocessor pin assignments and signal descriptions.



Signal Description

DB0 - DB7	Bidirectional data bus
ADDR0 - ADDR15	Address out
Φ Write	Clocks in
INT REQ	Interrupt request out
PRI IN	Priority in line
RAM WRITE	Write line out
EXT IN	External interrupt line in
REGDR	Register drive line
CPU READ	CPU read line out
ROMC0 - ROMC4	Control lines in
V_{ss} V_{dd} V_{gg}	Power lines

FIG. A.2.3-2. Fairchild F8 Memory Interface Chip pin assignments and signal description.

For extensions of the F8 System, where larger memory systems are employed, it's useful to be able to extend the triggering capability of the Model 100A. By connecting the Model 10 Trigger Expander to the appropriate points on the 3853 memory interface chip, the full 16-bit address bus may be monitored or used as a trigger source. The following tables describe the connections and control settings for the Model 100A and Model 10 analyzer system.

Model 10 Input Probes	3853 Monitoring Points
Ground	Vss or microprocessor ground
Clock	WRITE (pin 3)
D0-D7 data inputs	DBØ-DB7
AØ-A15 address inputs	ADDRØ-ADDR15
Q_0 (trigger qualifier)	$\overline{\text{RAM WRITE}}$
Q_1 (clock qualifier)	CPU READ

Model 10 and Model 100A Control Settings	
Model 10	
Display Multiplexer	data, upper address byte, lower address byte
Clock edge	negative-going
Q_0 (trigger qualifier)	"0" for write qualify, "1" for read
Q_1 (clock qualifier)	"1"
Delay select	clock or trigger delay
Delay set	0-999 as required
Address set	4-digit HEX address, as required
Address trigger mode	off or synchronous, as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	HEX
SINGLE/REPEAT	as required
POS/NEG TIME	as required
Trigger Switches	as required

This configuration permits triggering the Model 100A from any selected address point and/or data word in the F8 system. The trigger delay and read/write qualifiers are useful for stepping through a program as well as for program debugging.

A.2.4 LOGIC ANALYSIS OF THE SC/MP MICROPROCESSOR

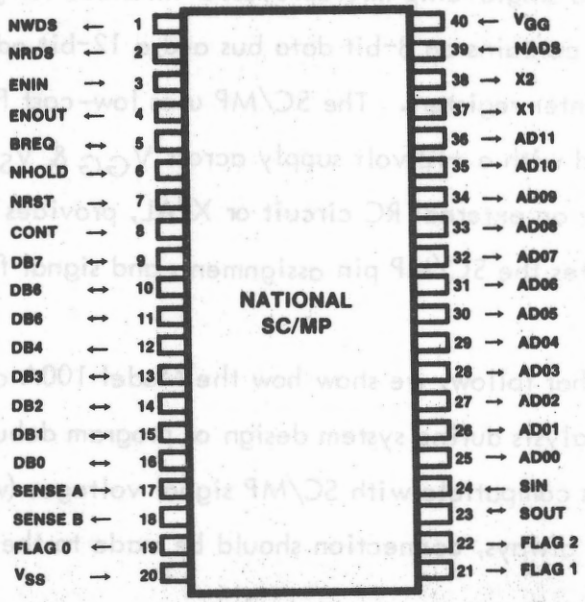
The SC/MP is a single-chip microprocessor intended for general-purpose control applications. The CPU contains an 8-bit data bus and a 12-bit address bus along with three auto-indexing pointer registers. The SC/MP uses low-cost P-Channel technology and is normally operated with a +12 volt supply across V_{GG} & V_{SS}. An internal clock generator, controlled by an external RC circuit or XTAL, provides the required timing. Figure A.2.4-1 illustrates the SC/MP pin assignments and signal functions.

In the tables that follow, we show how the Model 100A analyzer is to be connected to the SC/MP for analysis during system design or program debugging. Although the Model 100A analyzer is compatible with SC/MP signal voltages (when the 100A ground is connected to V_{GG}), as always, connection should be made to the buffered signals if they are available.

Model 100A input probes	SC/MP Monitoring Points
Ground	V_{GG} (microprocessor ground)
Clock	NRDS (pin 2)
D0-D7 (data inputs)	DBØ-DB7

Model 100A Control Settings	
Clock edge	positive-going
HEX/OCTAL	HEX
POS/NEG TIME	as required
SINGLE/REPEAT	as required
Trigger Switches	as required

With the above configurations, the Model 100A will monitor and display all SC/MP bus activity.



Signal Description

DB0-DB7	Data bus
AD00-AD11	Address bus
FLAGØ-FLAG2	User assigned, general-purpose bit
X1, X2	To external timing xtal/cap.
NWDS	Write strobe output
NRDS	Read strobe output
ENIN	Enable input
ENOUT	Enable output
BREQ	Bus request input/output
NHOLD	Hold lengthens input/output cycle
NRST	Reset input
CONT	Continue input
SENSEA-SENSE B	General purpose status inputs
NADS	Address strobe output
SIN	Serial input
SOUT	Serial output
V_{SS}	Positive supply voltage
V_{GG}	Negative supply voltage

FIG. A.2.4-1. SC/MP package configuration.

The Model 10 Trigger Expander extends the capability of the analyzer by allowing selectable, delayed triggering of any SC/MP system address. The following tables show how to connect the Model 10 and Model 100A into the SC/MP microprocessor system.

Model 10 Input Probes	SC/MP Monitoring Points
Ground	V_{GG} (microprocessor ground)
D0-D7 (data inputs)	DBØ-DB7
A0-A11 (address inputs)	ADØØ-AD11
A12-A15 (address inputs)	ground
Clock	NRDS (pin 2)
Q_0 (trigger qualifier)	ENOUT (pin 4)
Q_1 (clock qualifier)	not connected

Model 10 and Model 100A Control Settings	
Model 10	
Display Multiplexer	data, upper address byte, lower address byte
Clock edge	positive-going
Q_0 (trigger qualifier)	"1" for write qualify, "0" for read
Q_1 (clock qualifier)	off
delay select	clock or trigger delay
delay set	0-999, as required
address set	3-digit HEX addresses as required (Upper HEX digit = 0)
address trigger mode	off or synchronous as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	HEX
SINGLE/REPEAT	as required
POS/NEG TIME	as required
Trigger Switches	as required

This configuration allows you to monitor or trigger from the address bus or data bus of the SC/MP. The qualifier can be used to require a read or write operation to trigger the analyzer.

A.2.5 LOGIC ANALYSIS OF THE ZILOG Z-80

The Z-80 CPU is a third-generation, single-chip, microprocessor that is "upward compatible" with the INTEL 8080. The chip is fabricated using N-channel, silicon-gate, MOS technology and operates from a single +5 volt supply. All signals are TTL compatible.

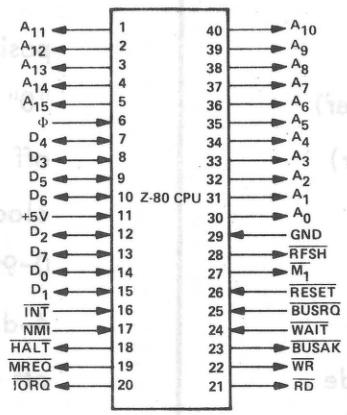
The Z-80 can operate at a 1.6 μsec instruction speed. Figure A.2.5-1 illustrates the Z-80's pin assignments and signal functions. The following two tables show the necessary connections and control settings for using the Model 100A to analyze the operation of the Z-80.

Model 100A Input Probes	Z-80 Monitoring Points
Ground	Vss or Microcomputer ground
Clock	ø
D_0-D_7 data inputs	D_0-D_7 data bus

Model 100A Control Settings	
Clock edge	positive-going
HEX/OCTAL	OCTAL
POS/NEG TIME	as required
SINGLE/REPEAT	as required
Trigger switches	as required

The above connections and control settings will permit the monitoring of the bus traffic to and from the CPU. If it is desirable to trigger the analyzer from a specific memory address while monitoring the data bus, then the Model 10 Trigger Expander can be added to the test set-up. The following tables indicate the required system connections and control settings for the Model 100A and the Model 10.

Model 10 Input Probes	Z-80 Monitoring Points
Ground	Vss or microcomputer ground
D_0-D_7 data inputs	D_0-D_7 data bus
A_0-A_{15} address inputs	A_0-A_{15} address bus
Clock	ø
Q_0 (trigger qualifier)	$\overline{WR}$



Signal Description

A_0-A_{15}	Tri-state address bus
D_0-D_7	Tri-state data bus
$\overline{M_1}$	Machine opcode fetch cycle
$\overline{MREQ}$	Memory request
$\overline{IORQ}$	I/O address valid
$\overline{RD}$	Memory read
$\overline{WR}$	Memory write
$\overline{RFSH}$	Refresh request
$\overline{HALT}$	Indicates CPU halted
$\overline{WAIT}$	Input to place CPU in wait state
$\overline{INT}$	Interrupt request
$\overline{NMI}$	Non maskable interrupt request
$\overline{RESET}$	CPU initialization
$\overline{BUSRQ}$	Request to CPU for control of address and data busses
$\overline{BUSAK}$	Acknowledge to external device for bus grant

FIG. A.2.5.-1. Zilog-80 CPU package configuration.

Model 10 and Model 100A Control Settings	
Model 10	
Display multiplexer	data, upper address byte, lower address byte
Clock edge	positive-going
Q_0 (trigger qualifier)	"0" for write; "1" for read
Q_1 (clock qualifier)	off
Delay select	clock or trigger delay
Delay set	0-999, as required
Address set	4-digit HEX address
Address trigger mode	off or synchronous as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	OCTAL
SINGLE/REPEAT	as required
POS/NEG TIME	as required
Trigger switches	as required

Thus, the settings and connections in the above tables permit the triggering of the Model 10 on a selected address occurrence. Note that the Q_0 qualifier may be used to trigger on either read or write operations.

A.2.6 LOGIC ANALYSIS OF THE RCA COSMAC

The COSMAC (CDP 1802) microprocessor is an 8-bit, one-chip, device which is fabricated using CMOS technology. It is designed to be used as a general purpose computing or controlling element in a wide range of stored-program applications.

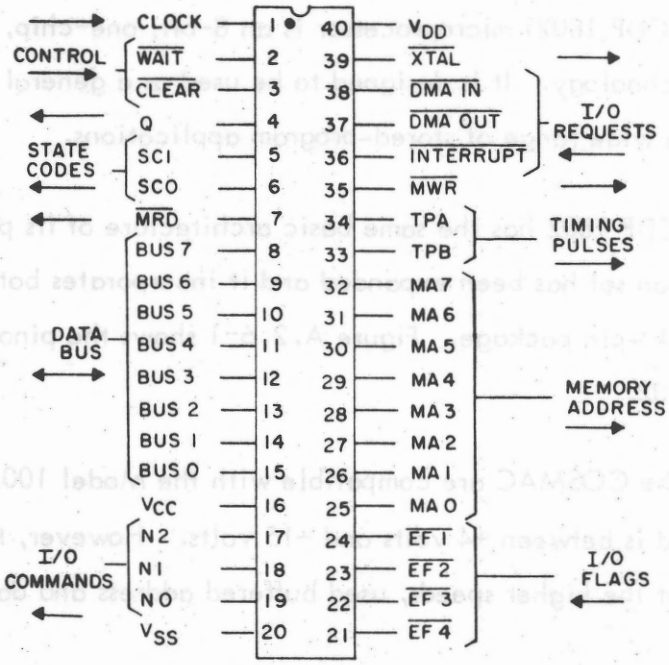
The COSMAC CDP 1802 has the same basic architecture of its predecessor, the CDP 1801, but its instruction set has been expanded and it incorporates both register and control functions in a single, 40-pin package. Figure A.2.6-1 shows the pinouts and signal descriptions of the CDP 1802.

All outputs of the COSMAC are compatible with the Model 100A's inputs as long as Vss is at ground and Vdd is between +4 volts and +15 volts. However, to avoid affecting microprocessor operation at the higher speeds, used buffered address and data busses, if possible.

The following two tables show the connections and control settings for analyzing the COSMAC microprocessor with the Model 100A.

Model 100A Input Probes	COSMAC Monitoring Points
Ground	Vss or system ground
Clock	TPB (pin 33)
D_0-D_7	BUS_0-BUS_7

Model 100A Control Settings	
Clock edge	positive-going
HEX/OCTAL	HEX
POS/NEG TIME	as required
SINGLE/REPEAT	as required
Trigger switches	as required



Signal Descriptions

CLOCK	External clock input
WAIT, CLEAR	Control mode inputs
Q	Single bit output
SC0, SC1	CPU state signals
BUS0, BUS7	CPU data bus
V_{cc}	Output pull-up rail
N0, N1, N2	I/O commands
V_{ss}	Most negative supply (ground)
V_{dd}	Most positive supply
XTAL	Crystal input for on-chip oscillator
DMA IN, DMA OUT, INTERRUPT	I/O request inputs
TPA, TPB	Timing pulse outputs
MA0, MA7	Memory address (multiplexed)
EF1, EF4	I/O flag inputs

FIG. A.2.6-1. CDP 1802 pinouts and signal descriptions.

With the connections and control settings shown in the previous tables, all COSMAC data bus activity can be observed. Thus, this is the set-up to use for basic system troubleshooting and software debugging. However, if the ability to trigger on a selected 16-bit address is required, then the Model 10 Trigger Expander can be added to the set-up. Note that the COSMAC utilizes a multiplexed address scheme which requires a latch to hold the upper 8 bits of the memory address. (The use of this latch is described in the application notes of the CDP 1802.) When using the Model 10, address inputs A_8-A_{15} should be connected to the latch outputs.

The next two tables describe the connections and control settings required when using the Model 10 with the Model 100A to analyze the operation of the COSMAC microprocessor.

Model 10 Input Probes	COSMAC Monitoring Points
Ground	Vss or system ground
Clock	TPB (pin 33)
D_0-D_7 (data)	data bus
A_0-A_7 (lower byte)	MA_0-MA_7
A_8-A_{15} (upper byte)	upper address latch outputs
Q_0 (trigger qualifier)	$\overline{MWR}$ (pin 35)
Q_2 (clock qualifier)	not used

Model 10 and Model 100A Control Settings	
Model 10	
Display Multiplexer	data, upper address byte, lower address byte
Clock edge	positive-going
Q_0 (trigger qualifier)	"0" for write qualifier; "1" for read
Q_1 (clock qualifier)	off
Delay select	clock or trigger delay
Delay set	0-999, as required

Model 10 and Model 100A Control Settings (con't)	
Address set	4-digit HEX address, as required
Address trigger mode	off or synchronous, as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	HEX
SINGLE/REPEAT	as required
POS/NEG TIME	as required
Trigger switches	as required

A.2.7 LOGIC ANALYSIS OF BIT-SLICE MICROPROCESSORS

Microprogrammed minicomputers, based on the popular bit-slice chips such as the AM2901, the INTEL 3002, and the SBP0400, are another example of complex digital hardware which can readily be analyzed using the Model 100A. Generally, these bit-slice chips contain several general registers, one or more working registers, and an arithmetic logic unit (ALU), and can be concatenated to form a minicomputer whose word length can be any practical multiple of two to four bits.

Figure A.2.7-1 is a simplified block diagram of a typical minicomputer based on a bit-slice microprocessor. Note the use of a microprogrammed control structure, which permits the user to define and implement his own instruction set. And since these chips are usually fabricated using TTL technology rather than MOS, their instruction execution times are at least an order of magnitude faster than the 8080-type microprocessor. Thus it's a matter of both speed and user flexibility when bit-slice elements are chosen for use in a minicomputer.

When using the Model 100A with a bit-slice minicomputer, one of the most useful monitoring points is the control memory address bus, which forms the address of the microprogram memory, and thus selects the microcontrol word. Then, with the input clock probe connected to the correct phase of the system clock, the user can trace the microinstruction sequence of the minicomputer. This ability is essential for debugging microprograms or even verifying the correct operation of an existing machine.

Additional analysis capability may be obtained by connecting the Model 10 Trigger Expander between the minicomputer and the Model 100A. Using this combination, the control memory address bus is connected to the address inputs of the Model 10. (Up to 16 are available.) The remaining data inputs of the Model 10 can be used to probe different sections of the minicomputer, as required. As an example, let's investigate the probe connections and control settings required to check out an 8-bit divide algorithm which we've just completed microprogramming.

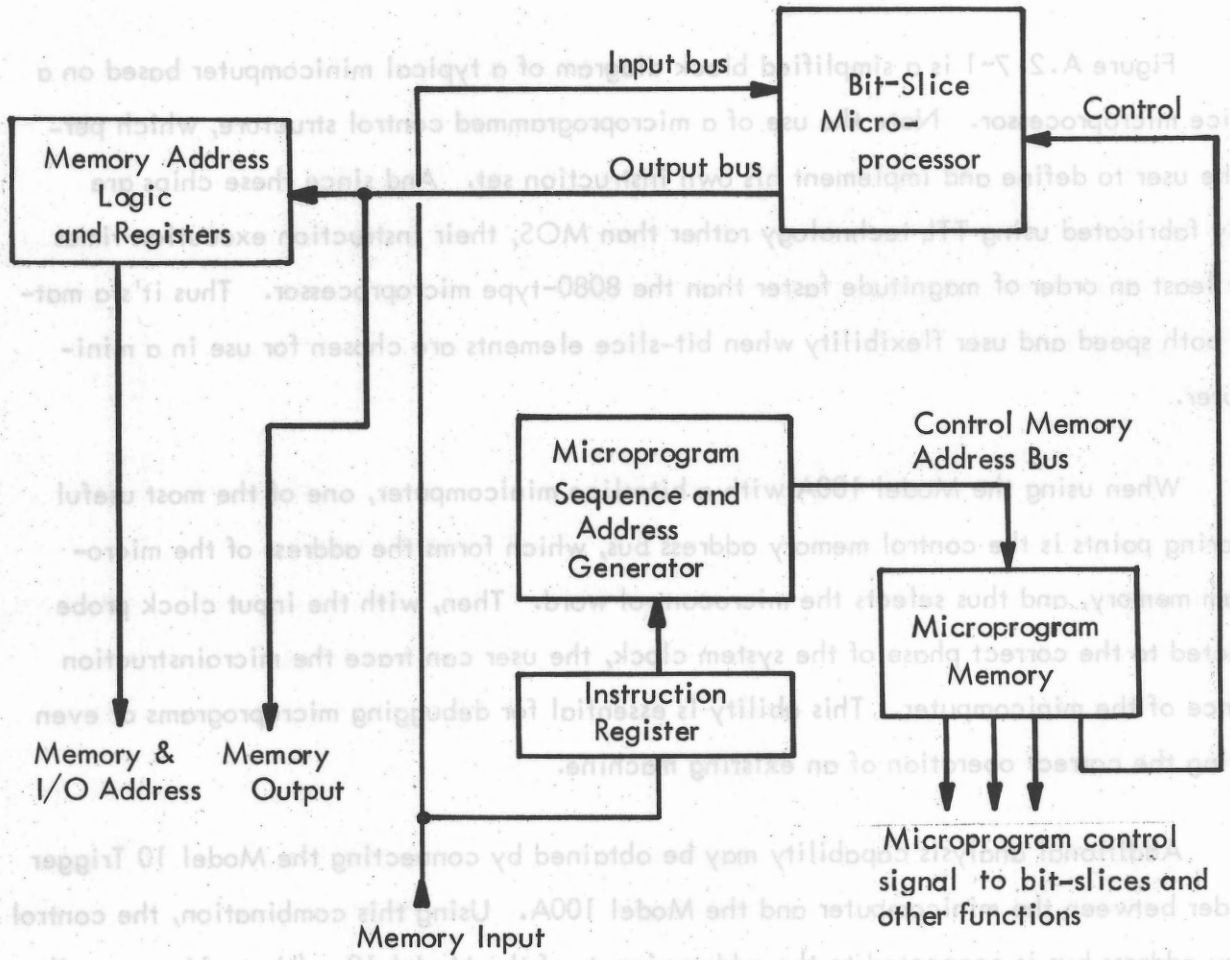


FIG. A.2.6-1. Basic bit-slice microprocessor computer block diagram.

Model 10 Input Probes	Bit-Slice Monitoring Points
Ground	system ground
D_0-D_7 (data inputs)	ALU output
A_0-A_{15} (address inputs) (ground unused inputs)	control memory address bus
Clock	system clock
Q_0-Q_1 (qualifiers)	not used

Model 10 and Model 100A Control Settings	
Model 10	
Address set	4-digit start of divide microprogram
Address trigger mode	synchronous
Clock	active edge of system clock
Qualifiers	off
Display multiplexer	data, upper address byte, lower address byte
Delay select	clock
Delay set	0-999, as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	as required
SINGLE/REPEAT	REPEAT
POS/NEG TIME	POS
Trigger switches	all "X"

With the above connections and control settings, place the minicomputer in a loop executing the divide instruction with a known set of operands. Set the display multiplexer to the lower address byte to view the steps of the microprogram, which has been previously prepared from a microflow chart. If the sequence is longer than 16 microinstructions, we can "walk through" the microprogram by simply increasing the trigger delay.

Now, by selecting the appropriate position of the display multiplexer, we can view the data at the output of the ALU for each microprogram step. And, by moving the data probes to the various control and status signals, we can view these signals as the divide algorithm is being executed.

Thus, in summary, the logic analyzer reduces microprogram development, debugging, and troubleshooting to a relatively straight-foward task. Without this unique instrument, the advanced, high performance machines now appearing on the market would be more costly--if not impossible--to develop.

A.3 PRODUCTION TESTING APPLICATIONS

The emphasis in production testing is on a thorough and rapid verification of product performance. For today's complex digital systems, this usually means collecting and processing as much data in parallel as possible. And as manufacturing companies become cognizant of the cost savings inherent in the utilization of logic analyzers for this purpose, these instruments are being integrated into more and more production test set-ups as permanent test fixtures.

Figure A.3-1 shows one simple--but effective--testing concept incorporating an analyzer. Here the Model 100A is connected to the system under test through a simple test adaptor which provides both the multiplexing and interfacing functions for incoming test data. The probes fanning out from the adaptor can be connected to the appropriate IC's in the system using IC clips, or to one or more connectors specifically incorporated into the system for production testing.

Through the use of simple inverting logic, where required, the test adaptor normalizes the polarity of the incoming system clock so that the operator need not change the clock edge select switch on the analyzer during the testing sequence. Additional logic can be included to condition the input data to reduce the number of truth tables that need to be monitored. And, if a ROM or other appropriate logic element is used, it is possible to translate the first data word in each truth table into a common trigger word. This approach eliminates the need for the operator to change the trigger switches during the testing sequence. In fact, if the Model 100A's REPEAT mode can be used for the automatic display of data, the only control that need be operated during the entire testing sequence is the data selector switch on the test adaptor.

Referring back to figure A.3-1, the test procedure would then be as follows:

1. Operator inserts a one-to-one negative of a reference truth table in the holder in front of the scope's CRT.

2. Operator selects switch position # 1, which corresponds to data probe # 1, on the test adaptor.

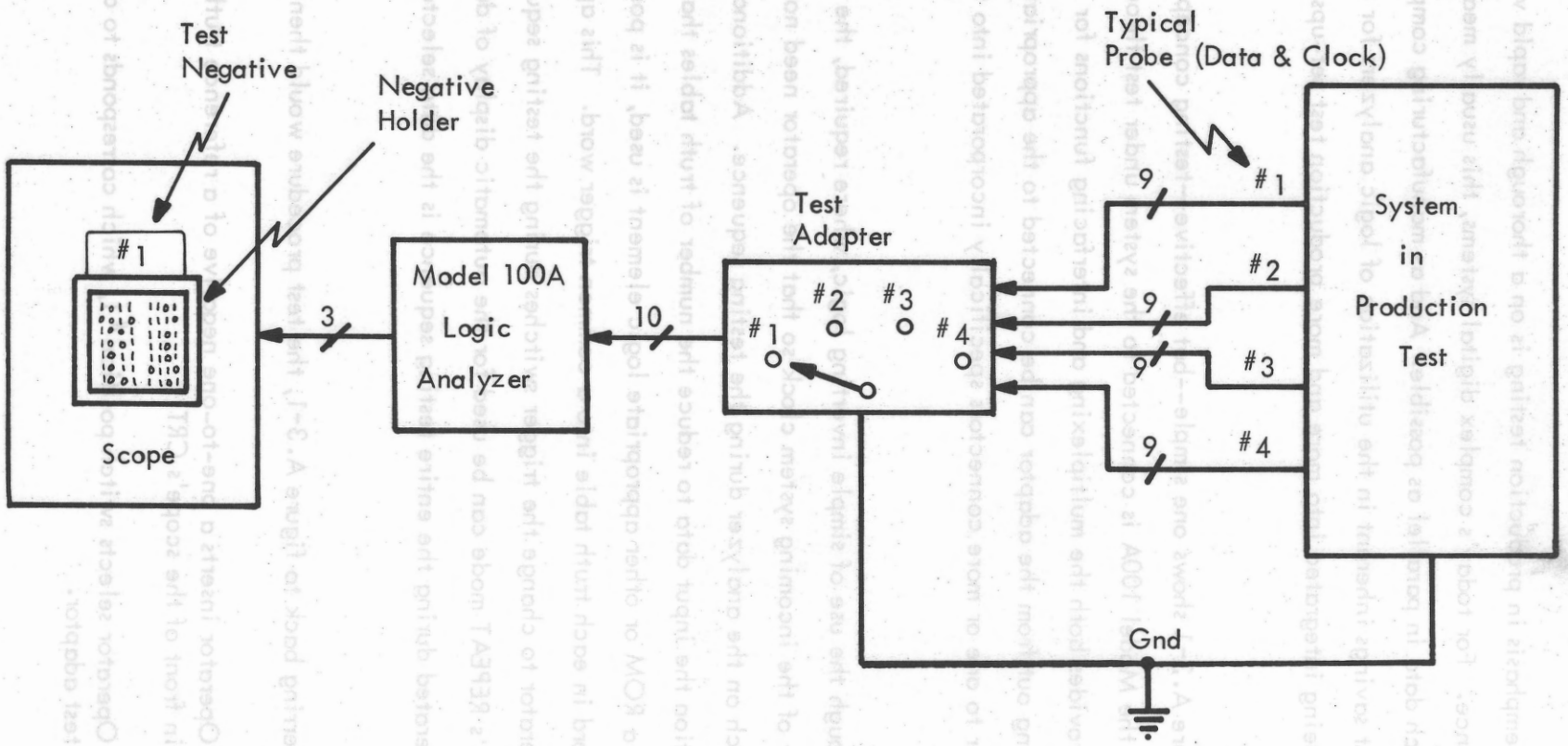


FIG. A.3-1. The test negative in front of the scope's CRT gives a rapid GO/NO GO indication for each truth table.

3. Resulting truth table either matches the negative--or does not.

4. If a match occurs, the test is continued. If there is no match, the faulty system is sent to the repair depot.

In the above example, note that over 500 bits of information can be reliably examined and verified in a matter of seconds. The only faster way to process this much information is to use an expensive dedicated processor or minicomputer.

Thus, for production testing applications, the Model 100A's main function is to collect and display as much critical information about the system as possible. And if the Model 10 Trigger Expander is included in the set-up (between the Model 100A and the system under test), the requirements imposed on the test adaptor can be significantly reduced.

A.4 FIELD SERVICE APPLICATIONS

In contrast with production testing, where the Model 100A is utilized primarily for its ability to efficiently collect and display large quantities of data, field service applications generally require the maximum use of the instrument's fault isolation capabilities. In addition, field service applications require that a test device be compact, light weight, and have low input power...characteristics which are common to the Model 100A.

For troubleshooting simpler digital systems, the analyzer can be connected to the appropriate IC's using a probe with one or more permanent IC clips wired-in at one end. For more complex systems, a test set-up, similar to the one shown in the last section, can be used. In either case, once the erroneous logic state is determined, the TRIG output of the analyzer can be extremely helpful in isolating the cause.

For example, assume that a timing component in a digital controller drifted slightly out of tolerance such that the clock at the input to a type D flip flop is occurring before the corresponding input data is completely stable. Thus, at times, the flip flop's Q output would be clocked to an erroneous state. After some preliminary testing, the field service engineer would be able to identify the area of the circuit that had malfunctioned by comparing observed truth tables with the reference tables (either by utilizing the test negative concept or printed truth tables in the maintenance manual).

However, without additional testing visibility, the engineer may not be able to rapidly identify the source of the problem. The Model 100A provides this additional visibility through the use of the TRIG output feature as shown in figure A. 4-1. (Recall that a sync pulse occurs at this output every time the pre-set trigger word appears at the input to the analyzer.) In the figure, the analyzer is providing a sync pulse to the scope at the occurrence of the faulty logic state. Hence, with some additional probing, the field service engineer can rapidly trace the source of the problem back to the clock.

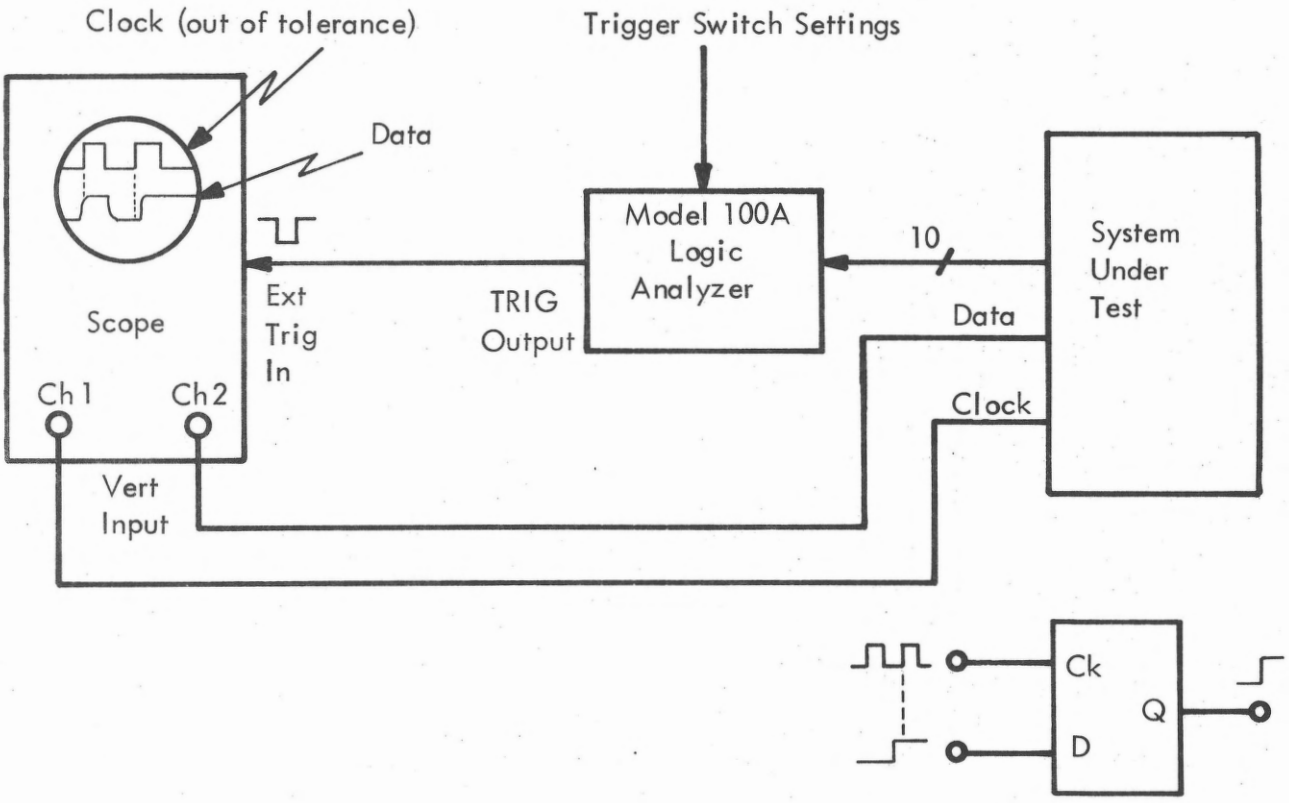
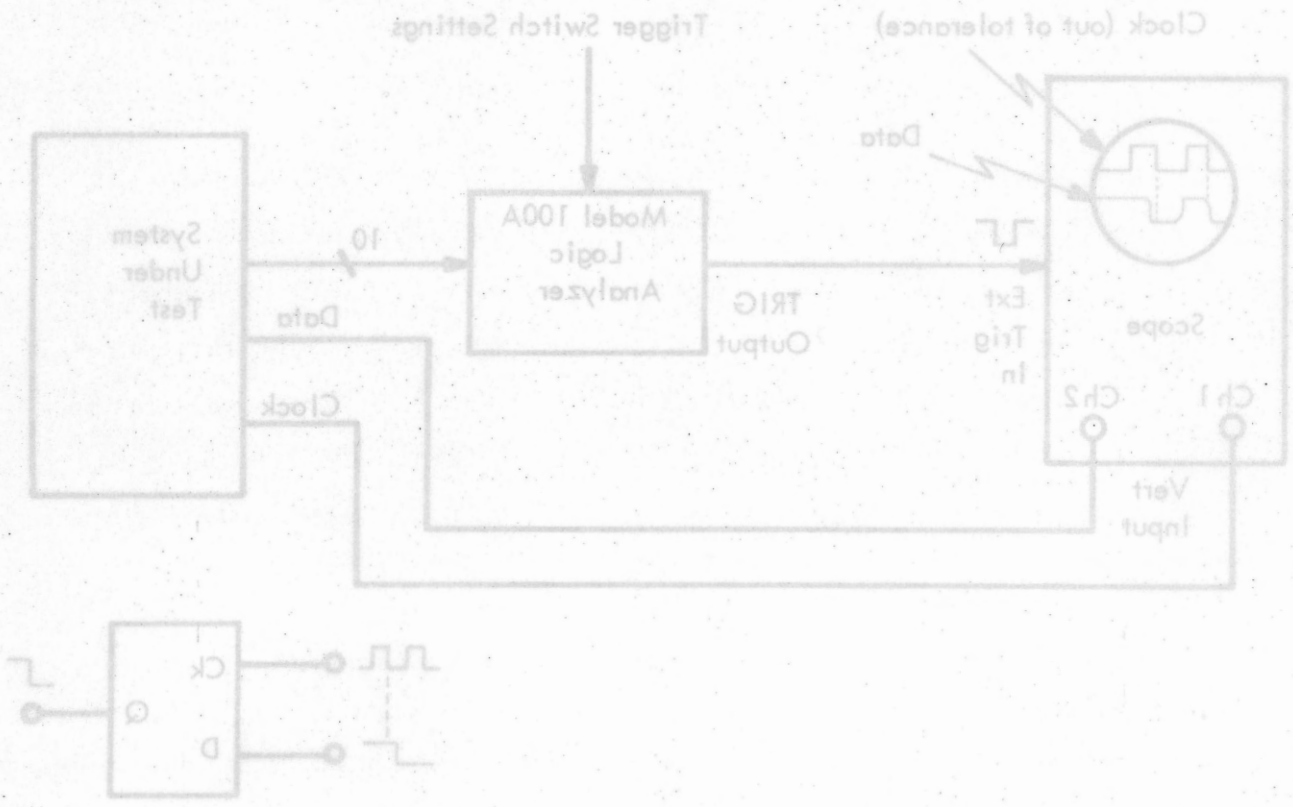


FIG. A.4-1. Using the TRIG output of the Model 100A for fault isolation.

As illustrated by this example, the Model 100A 's features permit the field service engineer to combine a digital troubleshooting technique (the capturing of an illegal logic state) with an analog technique (the use of the resulting TRIG output pulse to pinpoint a waveform timing problem). The use of these combined techniques provides the field service engineer with a powerful troubleshooting tool--the kind of tool required for maintaining the complex systems now being manufactured and placed in the field.



A.5 EDUCATIONAL APPLICATIONS

As we've stated before, the logic analyzer provides a unique window into the events of the digital world. And because of this, it makes an excellent educational tool. With an analyzer, electronics students at all levels can further their understanding of digital devices and systems: the flexibility and ease of use of the Model 100A encourages the student to find new ways to explore and comprehend the operation of his circuit.

With the advent of the logic analyzer, the name "data domain" was coined to describe the way the instrument operates on, and displays, digital events. Whereas the time and frequency domains are characterized by the mathematics of Laplace and Fourier, respectively, the data domain is governed by the rules of Boole and von Neumann.

In the data domain, events are considered to occur only at discrete intervals of time which are usually defined by the system clock. In fact, one does not normally care what happens in a digital circuit during an interval of time that does not contain an active clock edge. It is this fact which makes even the most complex digital circuit easier to understand. Thus, when a student of digital electronics creates or investigates a new circuit, he often finds it useful to think entirely in terms of "1's" and "0's." For example, he "knows" that a "0" at the output of a 2-input NAND gate is the result of two "1's" at the input; and that a 4-bit binary "down" counter can be preset to 0111--and "roll over" to 0000 after 7 clock pulses.

When thinking of circuits in these terms, the student is fundamentally constructing a portion of the truth table which fully characterizes the digital device. And, as we have shown throughout this manual, the logic (state) analyzer is entirely compatible with this view of the digital world. Below is a partial list of devices and concepts that can be better visualized by using an analyzer:

General Digital Logic

1. Comparing the differences between binary, decimal, and Johnson counters; teaching the binary counting system.

2. Illustrating the operation of flip flops and data storage registers.

3. Examining the contents of ROMS and Field Programmable Logic Arrays (FPLA's).

4. Demonstrating shift register operation.

Computers

1. Monitoring program counter sequencing, particularly during branch or jump instructions.

2. Tracing the states of the memory address bus, especially to observe address arithmetic operations.

3. Observing the flow of instructions and operands on the data bus during program execution; teaching hex and octal instruction formats.

4. Understanding I/O sequences and the associated control signals.

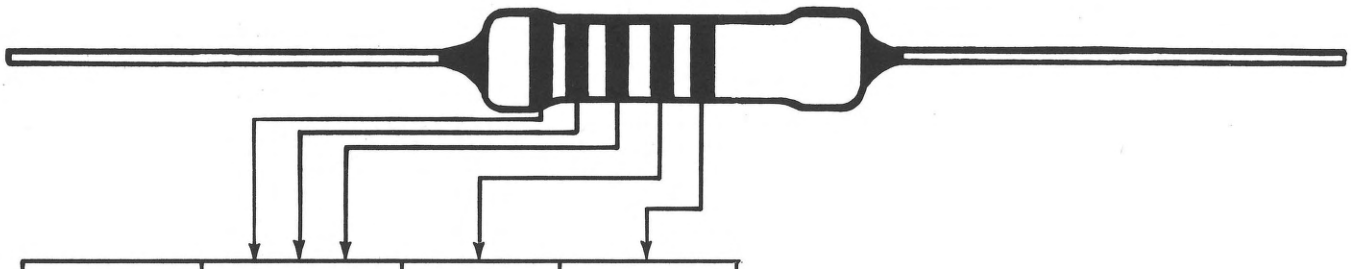
Microprogramming

1. Monitoring the address of the microprogram memory.

2. Observing the flow of microcontrol word sequences as macroinstructions are being formed and executed.

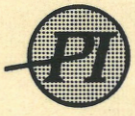
3. Understanding the functions of the various control and status signals used to form the branch address for the microsequencer.

RESISTOR COLOR CODING



Color	1st, 2nd, 3rd Significant Figure	Multiplier	Tolerance
Black	0	1	
Brown	1	10	±1%
Red	2	10^2	±2%
Orange	3	10^3	
Yellow	4	10^4	
Green	5	10^5	±0.5%
Blue	6	10^6	
Violet	7	10^7	
Grey	8	10^8	
White	9	10^9	
Silver		10^{-1}	
Gold		10^{-2}	±5%

1st band: digit
2nd band: digit
3rd band: digit
4th band: multiplier
5th band: tolerance



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